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OPTICAL JOINT TRANSFORM CORRELATOR.(U)
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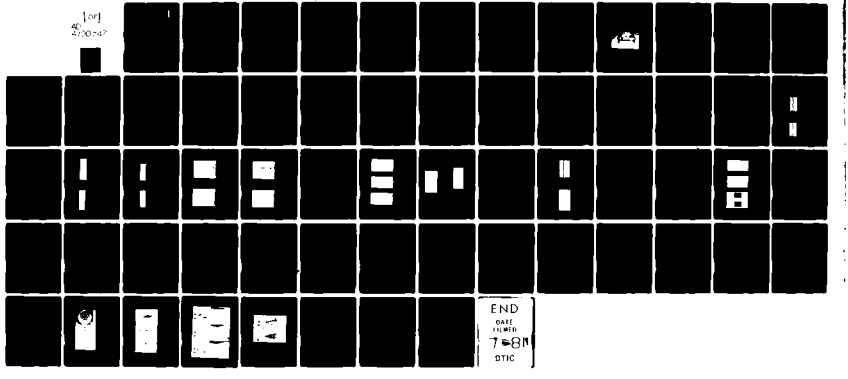

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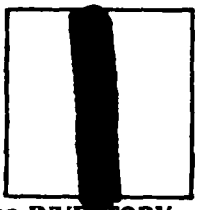

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Data Systems Div.

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Final Rept., 24 July 79 - 18 July 80. 26 Jan. 81

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DAAK40-79-C-0204

FINAL TECHNICAL REPORT

24 JULY 1979 - 18 JULY 1980

AMPEX CORPORATION
DATA SYSTEMS DIVISION

AMPEX

DAAK40-79-C-0204

OPTICAL JOINT TRANSFORM CORRELATOR

Ampex Corporation
Data Systems Division
401 Broadway
Redwood City, CA 94063

26 January 1981

Final Technical Report for Period 24 July 1979 - 18 July 1980

Prepared for

U.S. ARMY MISSILE COMMAND
REDSTONE ARSENAL, AL 35809
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Analysis Section

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20 ABSTRACT (Continue on reverse side if necessary and identify by block number)
The Joint Transform Correlator was built using a combination of optical components, analog electronics, and digital electronics. The optical system breadboard can be used to evaluate the correlation process and determine tolerance limits of the optical process. Correlation is achieved using a reference matched filter adjacent to the input image.

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1. INTRODUCTION

The optical signal processor shown in figure 1.1 is a picture of the joint transform correlator. The system configuration resulted from modifications of a radar optical signal processor which was built and evaluated for BMDATC under contract #DASG60-77-C-0010. This report describes only the modifications to the existing equipment and the development of support electronics systems. Subsystems which did not require modifications are covered in the reports to BMDATC under this

The joint transform correlator was designed and fabricated with lenses, mirrors, and liquid crystal light valves which were used in the radar correlator. The electronics systems which were used were selected to best fit their application to the joint transform system. Additional electronic support systems were designed and fabricated to best achieve a cost effective joint transform correlator system. Devices which were used in the previous system for high frequency operation such as the Bragg cells, radar signal generator, and the mode locked cavity dumped laser are not part of the joint transform correlator system.

The system was evaluated on a limited basis and the results of preliminary tests are included in this report.

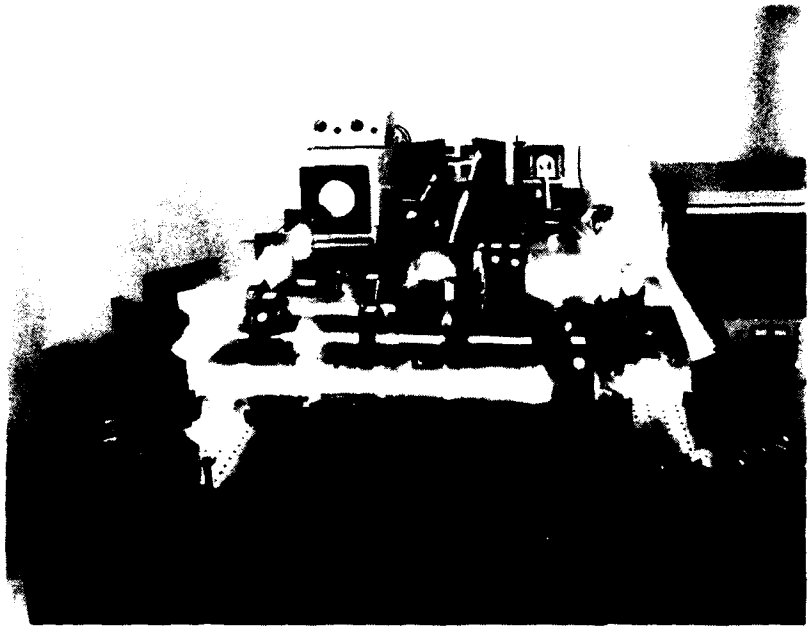


Figure 1.1 Optical Joint Transform Correlator

2. JOINT TRANSFORM CORRELATOR

2.1 BASIC SYSTEM CONCEPTS

There are several methods which can be used to optically correlate an input image with a reference matched filter. One method uses a holographic film for the matched filter at the transform plane. A second method uses adjacent input images which are spatially separated in the same plane. The images are illuminated by a coherent light source and a Fourier transform is jointly produced by a common optical system. The basic concepts of the joint transform correlator are illustrated in figure 2.1. Due to the nature of the optical system the Fourier transform from each image is overlapped with a one-to-one relationship. Areas of each of the produced Fourier transforms which have commonality will contain interference fringes. The interference fringe spatial frequency will be determined by the spatial relationship of the sources at the input plane of the joint transform correlator.

Producing the joint transform is the first of three basic steps which must be accomplished in order to obtain a system output. The second function of multiplication of the joint transforms is accomplished through a process of power detection. Power detection is accomplished by exposing photographic film placed at the joint transform plane. The film is then processed and placed back into the optical system. The processed film is then optically processed and a second Fourier transform is produced to achieve the system's output. A real-time system uses a spatial light modulator in place of the photographic film. The spatial light modulator is the power detector of the input optical system and the input transducer to the output optical system. The output of the spatial light modulator is again transformed by an optics system to produce the output correlation plane. The optical output of the system can be converted to an electrical signal and then digitized for further processing.

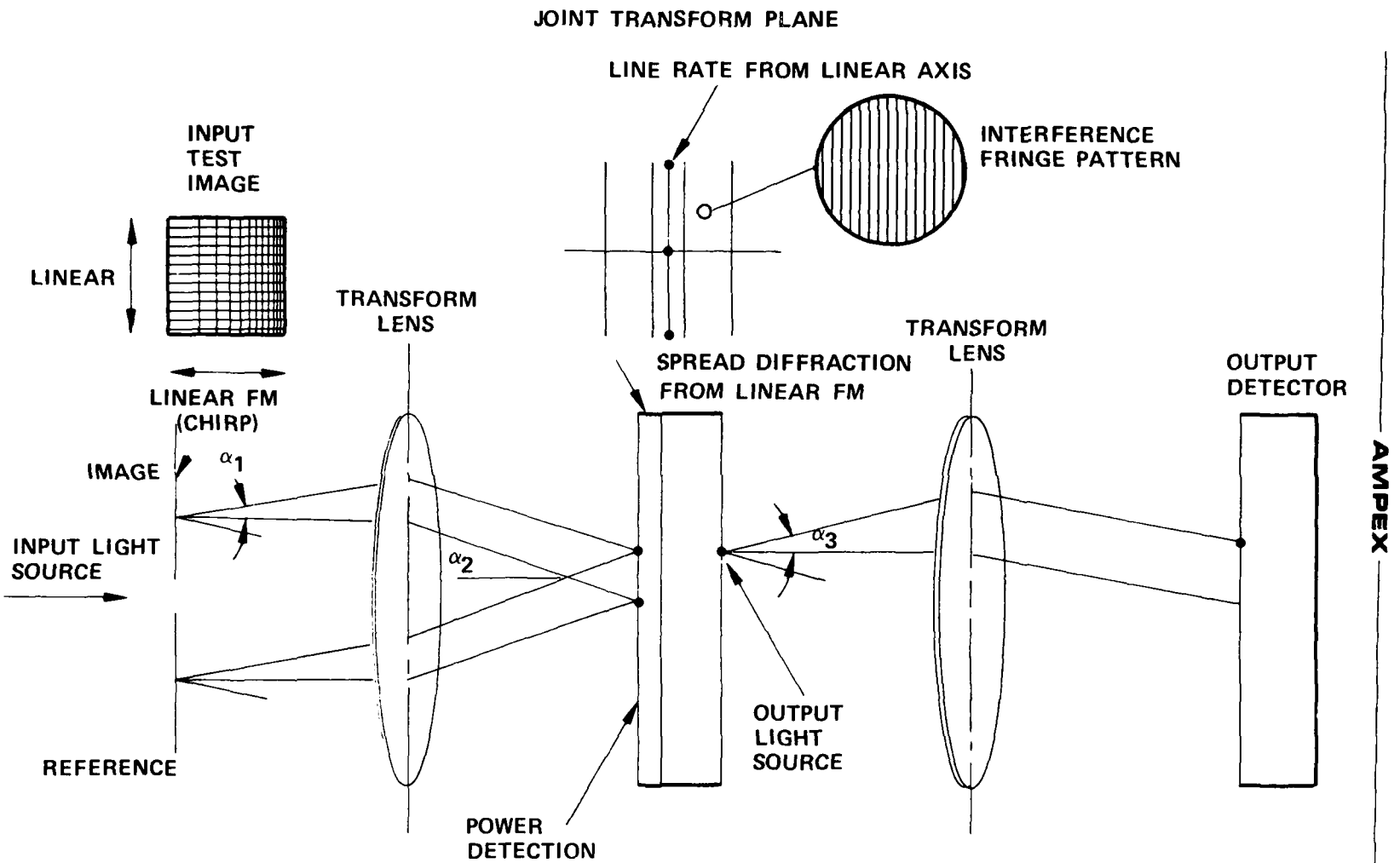


Figure 2.1 Optical Joint Transform Correlator

2.2 OPTICAL SYSTEM LAYOUT

A joint transform correlator system which uses modified television images for the input and implements optical spatial light modulators is shown in figure 2.2. The input images of the system are provided by a high resolution cathode ray tube which is imaged onto a liquid crystal light valve. The light source of both the input system and the output optical system is provided by a single laser. The light from the laser is divided into two paths. The upper path light source is collimated by the combination of a microscope objective and the collimating lens A1. The collimated light is used as the read light source for the input liquid crystal light valve. A Fourier transform of the liquid crystal light valve is produced by lens A3 where a spatial filter is used to remove the DC term (zero order). Lens A4 retransforms the optical information where a spatial filter is used to remove the sinc function produced by the input aperture. The joint optical signal is then retransformed at a second liquid crystal light valve where the cross- correlation terms are multiplied. The output of the second light valve is then processed by a method similar to the input optics system where the DC terms and the input aperture sinc functions are filtered. The input light to the output optics system is beam-formed through a microscope objective and the collimating lens pair A6,A7.

2.3 CATHODE RAY TUBE SYSTEM

The input transducer to the joint transform correlator is a system using a high resolution cathode ray tube working with a Hughes liquid crystal light valve. The electronics support system for the cathode ray tube is shown in figure 2.3. The electron beam is centered in the gun apertures by a magnetic field produced by the first centering coil. A second centering coil is used to center the undeflected beam at the center of the tube's faceplate. A magnetic lens composed of several coils is used to provide dynamic/static focusing and dynamic/static spot astigmatism correction. The deflection of the spot to produce a raster scan is also accomplished magnetically.

The cathode ray tube phosphor is protected in the event the circuits

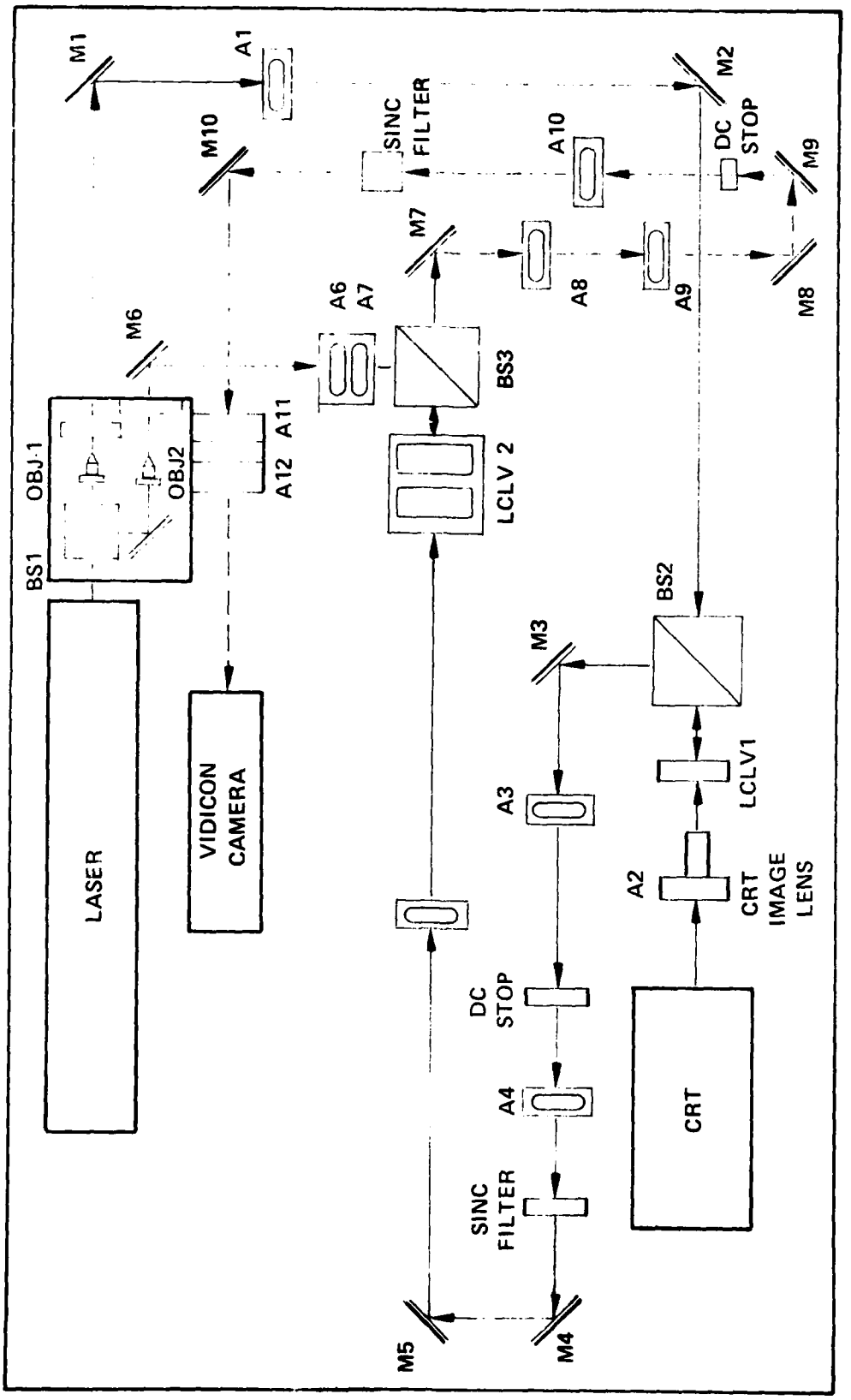


Figure 2.2 Joint Transform Correlator Optical System Layout

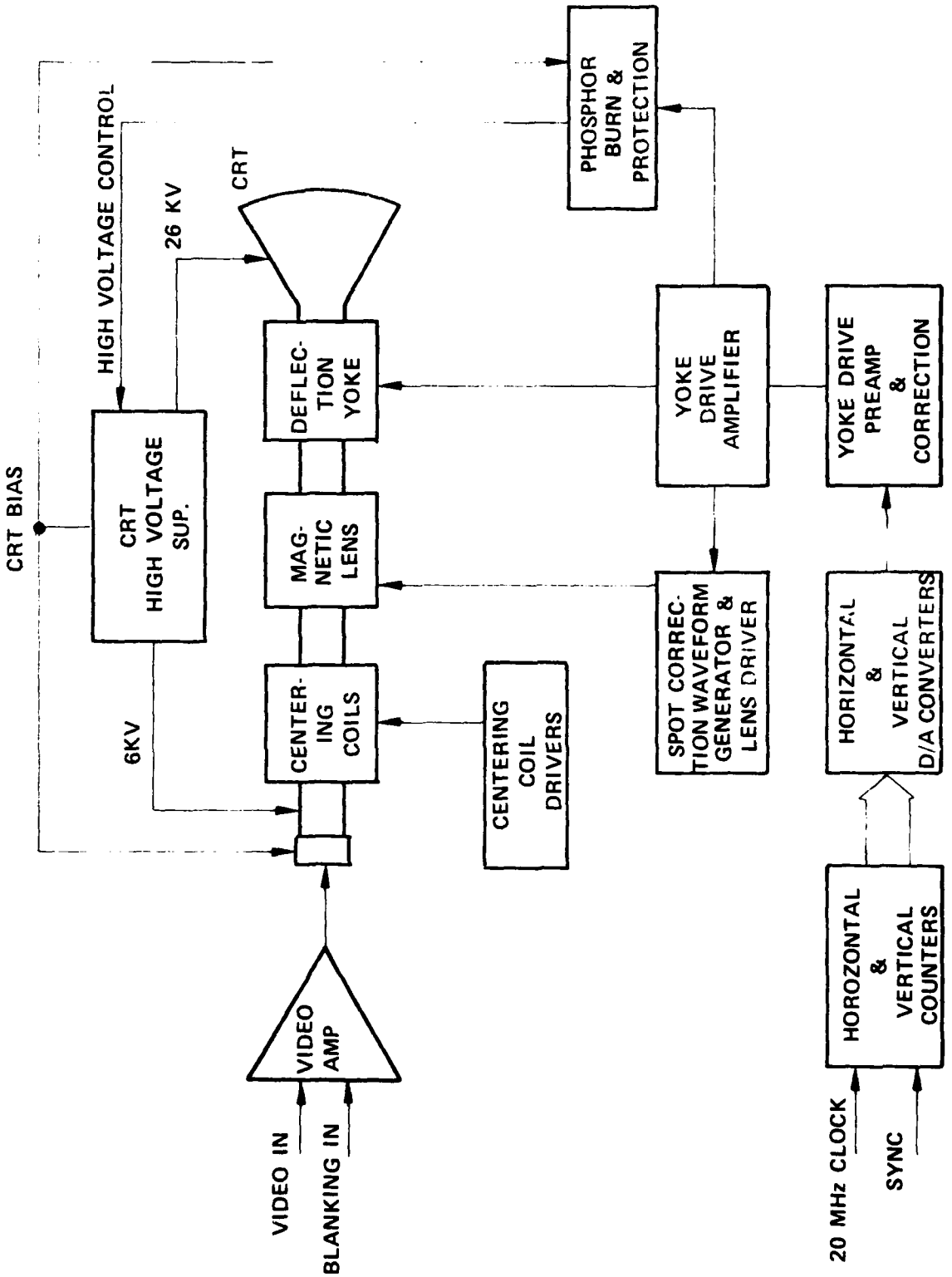


Figure 2.3 Cathode Ray Tube System

supporting the deflection and the control grid bias become defective. A detector system is used which senses the presence of the deflection waveform and the level of the bias to the cathode ray tube's control grid. The output of the detection circuit controls the positive bias and beam accelerating voltage in the event of a system failure.

The input to the cathode ray tube, provided by a video amplifier, is used to intensity modulate the electron beam. The input signal is to the cathode of the tube, thereby producing a brighter image element as the signal is driven in a negative direction.

To provide the necessary spatially separated images to the joint transform correlator, the vertical input waveform is modified. The video input signal to the system is a standard 2-to-1 interlaced signal which under normal scan conditions would produce a single image. If each field of the image is written with a modified vertical sweep, the fields will be spatially separated. Figure 2.4 demonstrates the vertical scan modifications which were used to obtain the spatially separated images. The vertical ramp is digitally generated and has a time base equivalent to a single frame. The two video fields will be written one above the other. However the spatial separation of the fields is not compatible with joint transform correlation until a square wave of appropriate amplitude and phase is added to the deflection waveform. Since each of the fields can contain independent video information, it is possible to obtain cross-correlation between the input image and a reference matched filter.

2.4 OPTICAL SYSTEM

The primary purpose of an optical system is to relay light from the system's input to the output. The optics system can be used to scale, rotate, and otherwise modify the light contained in the optical path. Spatial light modulators are used to modify the optical path in a predictable manner. Spatial filters are used to enhance the desired characteristics and eliminate undesired components from the optical path. One characteristic of a lens is to bring to near field the Fourier transform of the input function. The optical system with spatial light modulators can produce Fourier transforms, convolution, and correlation.

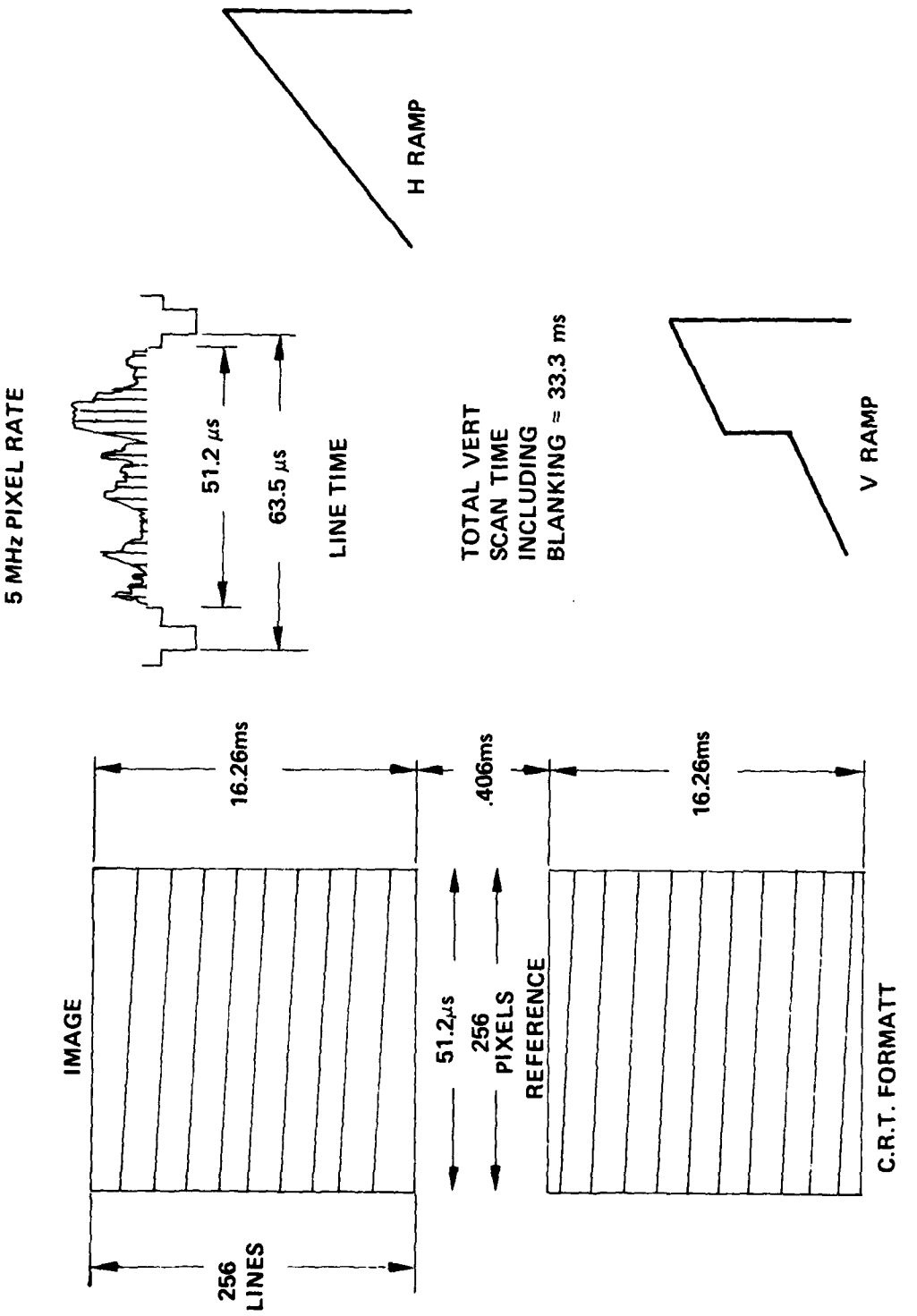


Figure 2.4 Cathode Ray Tbue Format

A schematic representation of a joint transform correlator is shown in figure 2.5. The cathode ray tube provides the joint image input to the system in a raster format, where each image is spatially separated. The joint images are written onto a liquid crystal light valve through the CRT image lens. The read light source (not shown) is provided through a polarized beam splitter. The cathode ray tube with the liquid crystal light valve introduces a complex diffraction grating to the optical system. The grating diffracts light at angles proportional to the wavelength of the light source and indirectly proportional to the spacing of the image elements. The first lens shown in figure 2.5 produces a Fourier transform of the joint images in the near field. Image components which have the same spatial frequency characteristics will be overlapped at the Fourier transform plane.

When two coherent light sources overlap having a defined angle of interference, fringes are produced. The distance between fringe peaks is directly proportional to the wavelength of the light source and indirectly proportional to the angle of interference. Therefore image elements from a common image plane which produce the same spatial frequency components at the transform plane will produce interference fringes which have a maximum frequency determined by the maximum distance of separation which can be achieved within an image aperture. The distance of separation between the image elements determines the interference angle at the transform plane. The elements which are common between the spatially separated images will inherently have a higher spatial interference frequency at the transform plane. Since the cross correlation fringe pattern has a higher spatial frequency than the crosscorrelation terms from a single image, it is possible to optically separate the crosscorrelation terms at the system output.

The spatial filter used at the first transform plane removes the DC term from the optical path. The diffraction efficiency of the optical spatial modulator is low and the majority of the light is contained in the DC term. This light is removed to prevent damage to the system's second liquid crystal light valve. The light is then retransformed by lens 2 to reform the joint image plane. The reimaged light is spatially filtered to remove the sinc function which is introduced to the optical system by the

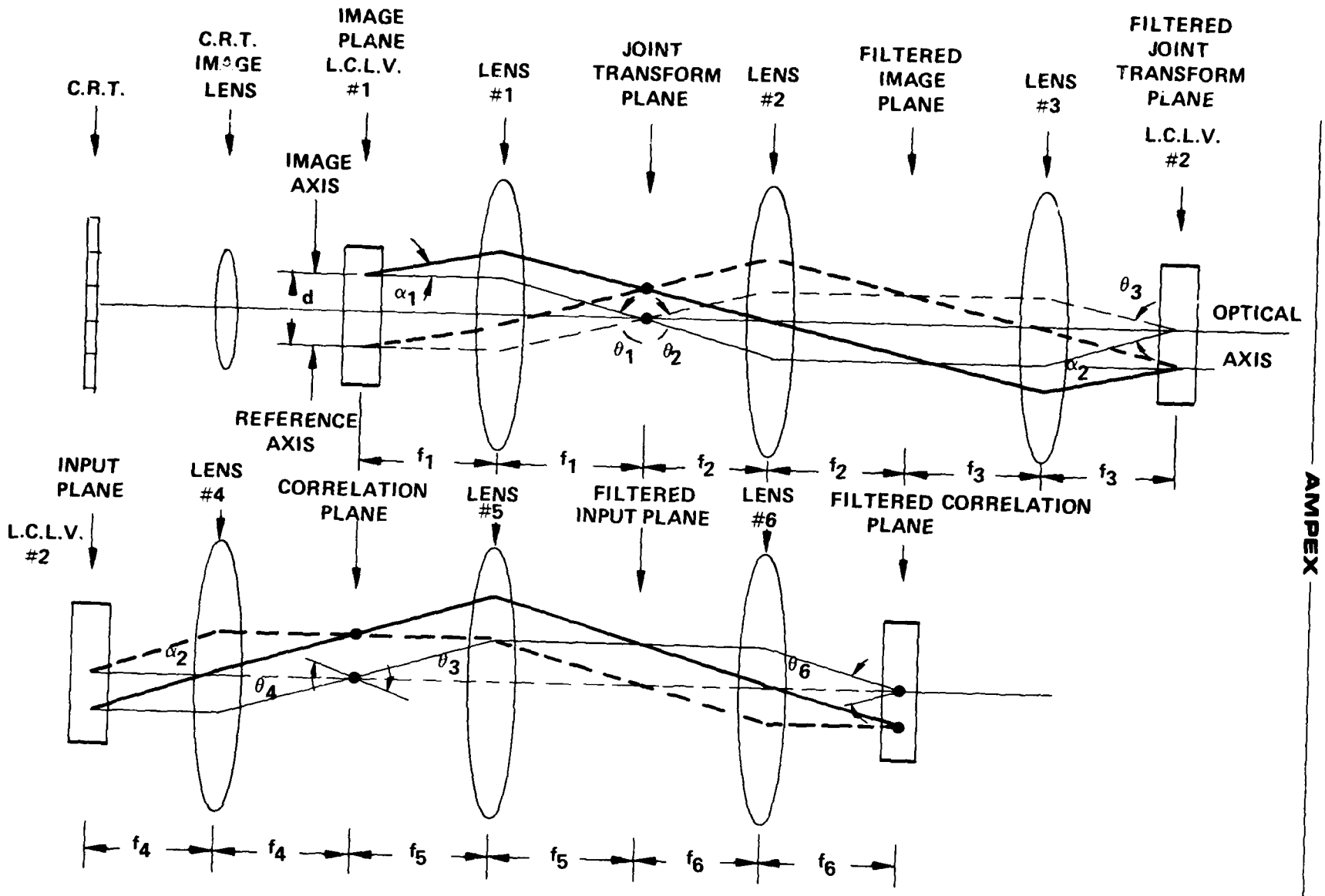


Figure 2.5 JTC Optical Schematic

input aperture. The sharp edges of the input aperture produce diffracted light, which, when transformed at the frequency plane, forms bright lines of light which are passed through the zero order (DC TERM). These edges are filtered after the DC term has been removed from the optical path. The reconstructed image has a dark center area and brightly illuminated edges. The bright edge information at the image plane is the sinc information which is filtered spatially before the light is retransformed onto the second liquid crystal light valve where power detection of the joint transform takes place.

The second light valve placed at the filtered joint transform plane has written onto it the complex frequency spectra from each of the spatially separated images. Since the common components of each image form interference fringes which become diffraction gratings for the read-out light, it becomes easy to see how the crosscorrelation terms can be separated at the system's output. The crosscorrelation terms having the higher spatial frequency can be high-pass filtered at the first transform plane at the same time the DC term is removed. The spatial high-pass filter will remove random terms as well as autocorrelation terms produced from a single input image. The output optical path is spatially filtered to prevent the DC term and the input aperture sinc function from damaging the system's output transducer.

3. THEORY OF OPERATION

3.1 JOINT TRANSFORM CORRELATOR SUPPORT SYSTEM

Figure 3.1 is a block diagram of the joint transform correlator support system which shows the subsystems which work together to provide the necessary operating functions inclusive of the cathode ray tube drive system, the frame store system, and the supporting computer system.

The electronic support system of the joint transform correlator is centered around a frame store memory and memory controller system. The memory is controlled in such a way as to provide either an analog image input to be stored in either video field, or the memory can be loaded from digital tape through the minicomputer system. It is not possible with the present controller to simultaneously load from the minicomputer and refresh the high resolution cathode ray tube system.

The analog input to the system is digitized with an 8-bit A/D converter and becomes the source of the Tri-State bus with interconnections to the frame store, D/A converter, and the computer interface. The output of the D/A converter provides the analog signal to the cathode ray tube system to enable monitoring of the input video signal. A single field of the video signal can be stored in memory and the memory when read will refresh that field to the cathode ray tube while the other field is displaying the live information. Digitized video which is stored in the memory system can be transferred to the minicomputer system through the computer interface. This process takes approximately 3 seconds. Once the digitized video is stored on the mini disk system it can be transferred through core to the digital tape system. Previously digitized video information can be transferred from the system's magnetic tape drive to the frame store where the frame store will be used to refresh the cathode ray tube system.

When an analog video system is used as the signal source, the system's synchronization is dependent on the video signal's timing. If the video is standard EIA composite video, the sync can be stripped and used as the sync source. Provisions have been made to synchronize the system with an optional composite sync input. The system's high frequency

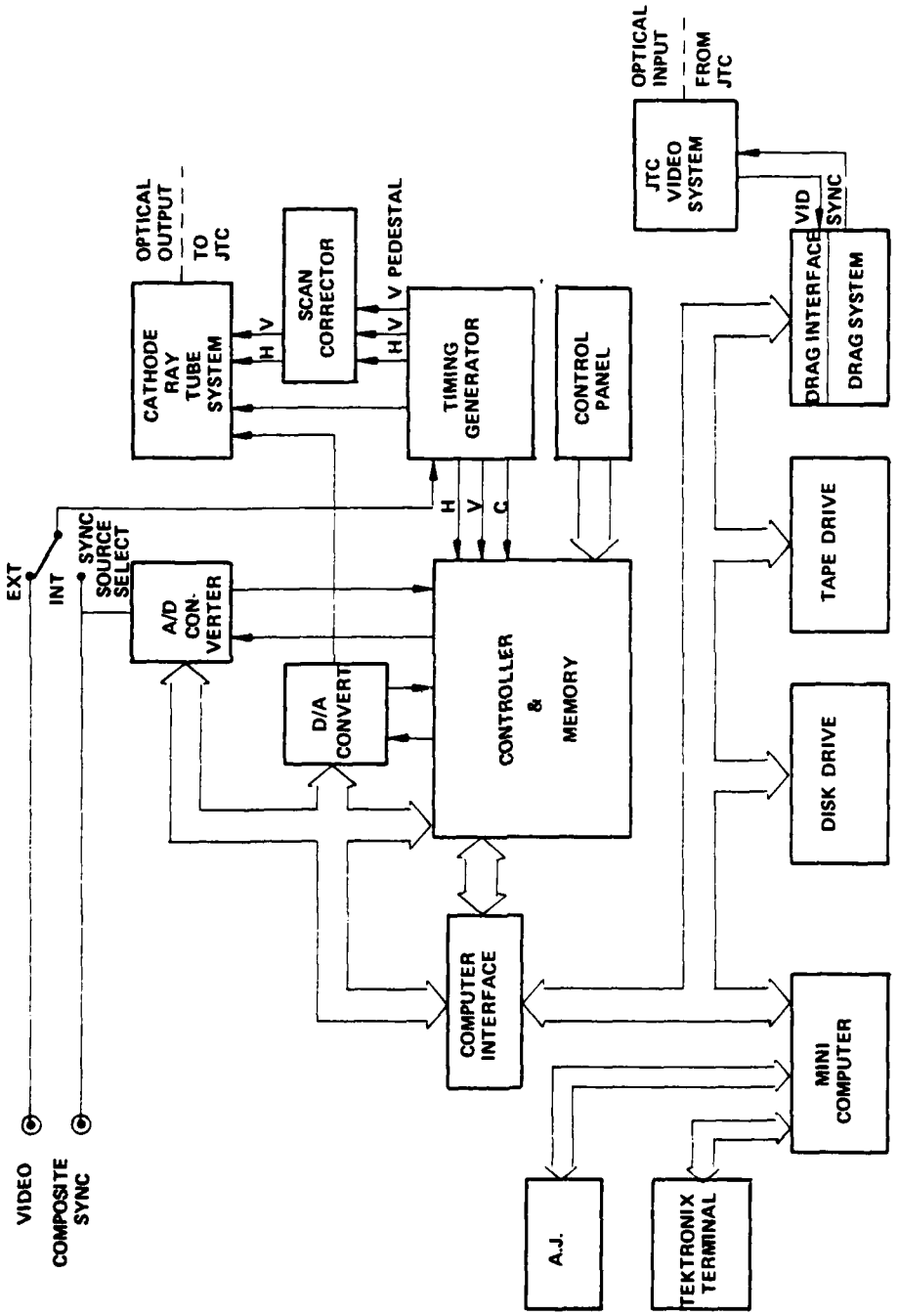


Figure 3.1 JTC Support System Block Diagram

clock is provided through the use of phase-lock loops. When the system is not externally synchronized, the system internal clock is automatically selected. When the system is running on internal clock all synchronizing and blanking signals are internally generated.

The sweep waveforms which are provided to the cathode ray tube system are digitally generated. When external sync is used, the sweeps are controlled accordingly so as to produce a stable image at the CRT.

A manual control panel has been provided so that images can be manually selected and stored. The video to the CRT can be selected from this control panel to provide the CRT with any combination of stored or live video input. Provision at the panel allows video signals to be stored in either or both fields.

3.2 FRAME STORE CONTROLLER

A block diagram of the frame store controller is shown in figure 3.2. As shown in the figure, the memory system is divided into two parts, each section storing 256 by 256 by 8 bits of digital video information. The input signals to the memory system include a 7-bit multiplexed address bus, row address select (RAS), column address select (CAS), in/out control (R/W), and the Tri-State video bus. All of the control lines to the memory are Tri-Stated so that separate sources can be used for memory control such as the frame store memory sequencer and the mini memory sequencer. It is the purpose of the sequencers to provide proper timing of the addresses with the appropriate strobe signals. The minicomputer has priority of control when selecting the sequencer which is to be used although a manual override has been provided.

The frame store when used to refresh the cathode ray tube does not require a refresh since the address generator cycles through all 128 row addresses within the time limits imposed by the dynamic memory integrated circuits. However, when the minicomputer is in control, it is necessary to use a refresh clock system which is transparent to minicomputer functions. The refresh is made transparent since all the data from the computer is latched. If the system is refreshing, the completion of the refresh cycle initiates the mini memory sequencer. When the memory

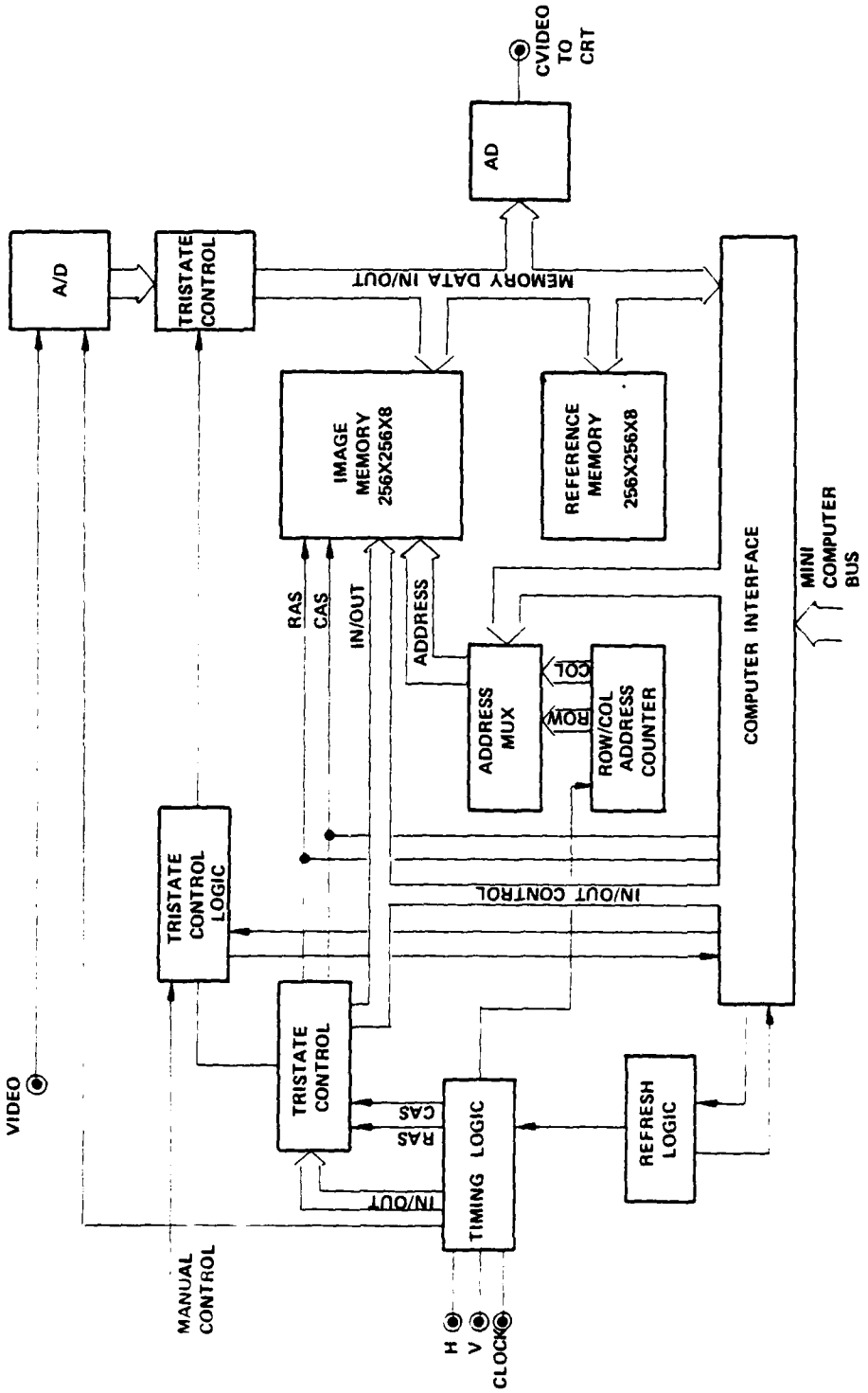


Figure 3.2 Block Diagram Memory Control System

sequencer is cycling through its functions and a refresh is required, refresh will be initiated upon completion of the cycle.

3.3 INPUT VIDEO PROCESSING

Figure 3.3 is a block diagram of the input video processing system. The input video is buffered, low-pass filtered, and passed to a video amplifier to the A/D converter. The filtered video is also used as an input signal for the sync stripper when internal synchronization is desired. The digitized video signal then becomes an input source to the video Tri-State bus when selected by the Tri-State control logic. The analog video level to the A/D converter can be adjusted with an on card control.

The A/D converter used in the system is a TRW TDC1007J. The circuit operates from +5 and -6 supplies and dissipates 2 watts. The digital inputs and outputs are fully TTL compatible, although except for the I/O buffers, the circuitry is Current Mode Logic and Emitter Follower Logic and operates from the -6 V supply alone. The nominal input range is 0 to -2 V, and a maximum of 30 ma is required through the reference resistor.

The A/D circuit operates over a guaranteed range of 0 to 20 MSPS with a typical maximum conversion rate of 30 MSPS. Performance has been achieved under controlled conditions at rates greater then 50 MSPS. The chip will accept an input signal with frequency components of up to 7 MHz and convert accurately without a sample and hold circuit. For multiplexed data or higher input bandwidth signal applications using an external sample and hold, the converter will recover from a full-scale step input within 20 ns.

3.4 SYNCHRONIZATION

Synchronization of the frame store with respect to the incoming video signal becomes critical when the input video source is a tape recorder without time base correction. Since the video can be slipping in time due to the recorder transport characteristics, it becomes necessary to produce timing signals to the memory which will track the time variations.

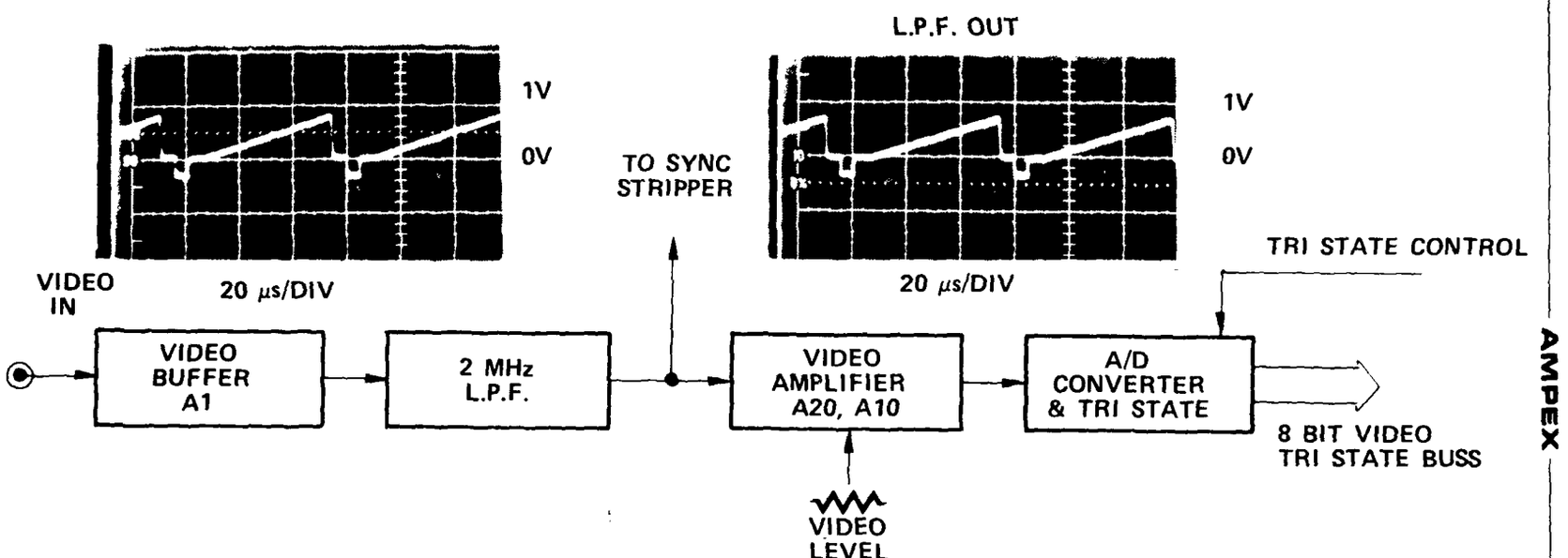


Figure 3.3 Input Video Processing

If the input signal is EIA composite video, the sync signals can be stripped from the video or an external composite synchronizing signal can be used. Figure 3.4 is a block diagram of the circuit which is used to process the synchronization information from the incoming video. The video from the low-pass filter is amplified by A41 and A42. The signal from A42 forms one input to an amplitude comparator. The other input to the comparator could be a DC reference level adjusted so that only the negative excursions of the sync produce a comparator output. However, it was anticipated that variations in the video signal black level from external noise or 60 Hz ground loops would produce instability in the output sync. A tracking reference level circuit is used which senses low frequency variations in video black level and adjusts the comparator reference voltage accordingly. The output of the comparator, shown in figure 3.4 was taken during the vertical intervale to demonstrate the timing of the equalization pulses.

The composite video signal is used to drive a non-retriggerable one-shot (A71) having a time constant of greater than 1/2 line period. Since the equalization pulses do not retrigger the one-shot, the horizontal drive signal is obtained, as shown in Figure 3.5.

The separation of the vertical synchronization signal from the composite synchronization signal could be accomplished by using an integrator and a comparator circuit. However, the integration technique would introduce the possibility of pulse jitter in the output.

The vertical drive signal equalization pulses are detected by using a one-shot and a gate. The one-shot is a retriggerable device which generates a stream of horizontal pulses except during the vertical interval due to the half line rate of the equalization pulses. The output of the one- shot is gated with composite sync to produce the string of vertical equalization pulses as shown in figure 3.6A. A one-shot (A92) is used to form the vertical blanking pulse as shown in figure 3.6C.

After the vertical blanking pulses have been detected it is possible to generate a pulse every even or odd field. Gate A72 has as one input the composite sync.signal while the other input is derived by logic from the detected vertical blanking signal. Figures 3.6B and 3.6D show the two

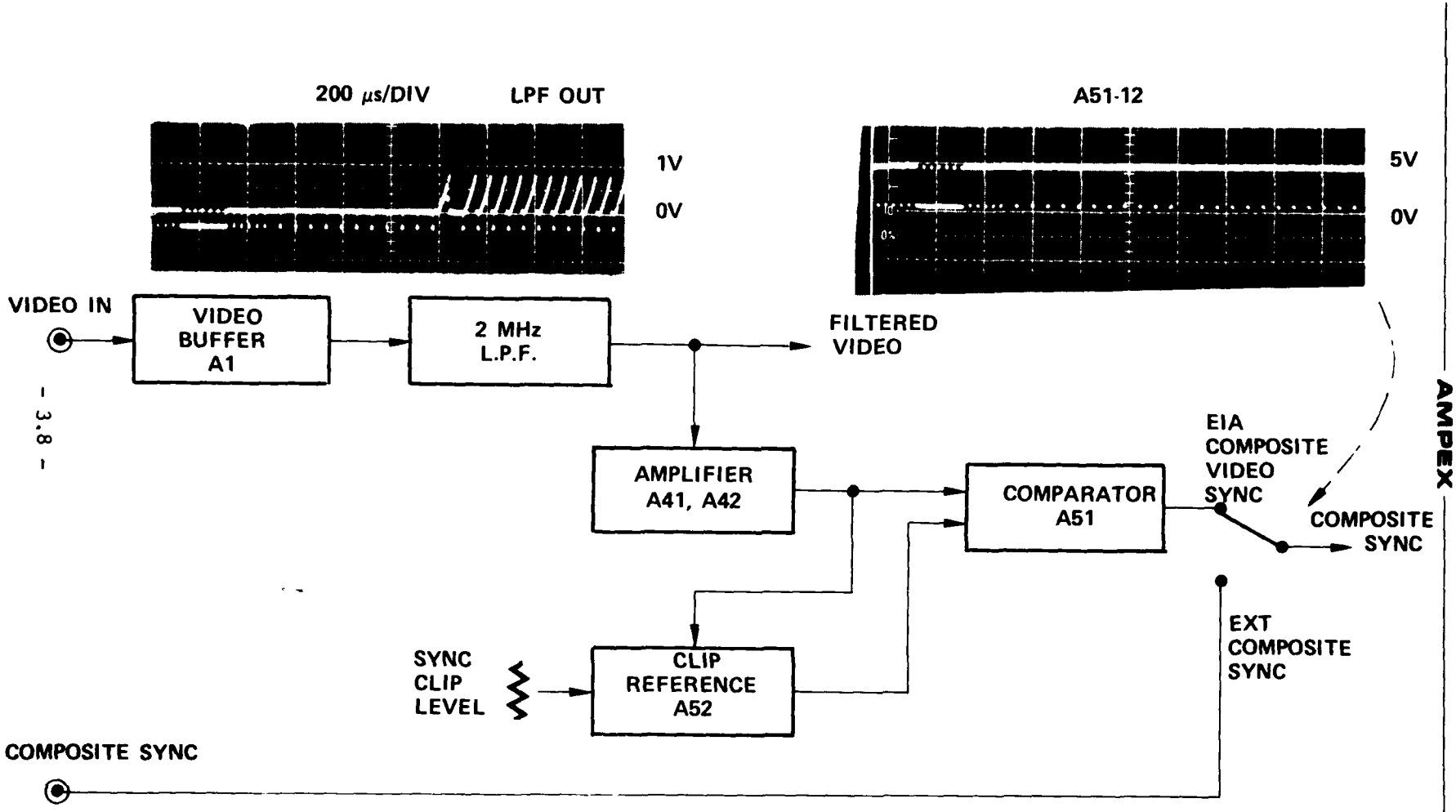


Figure 3.4 Sync Stripper

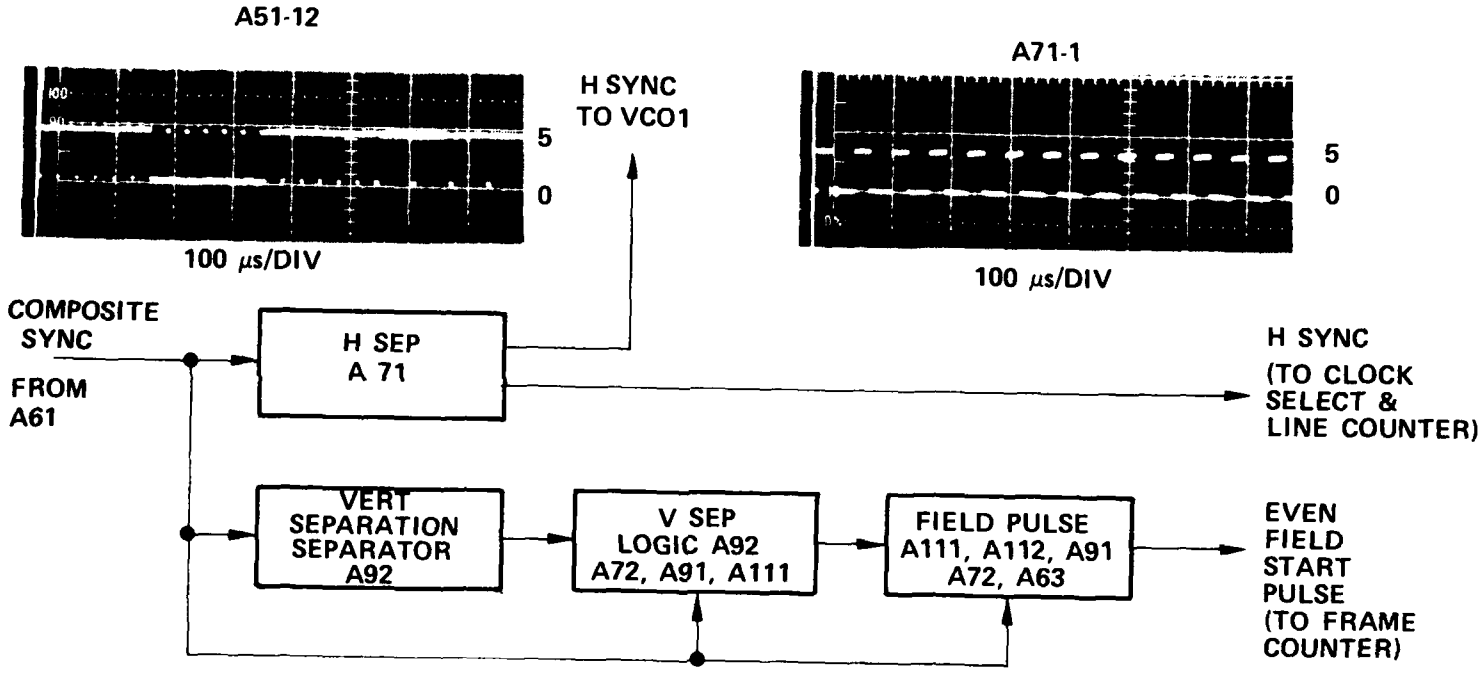
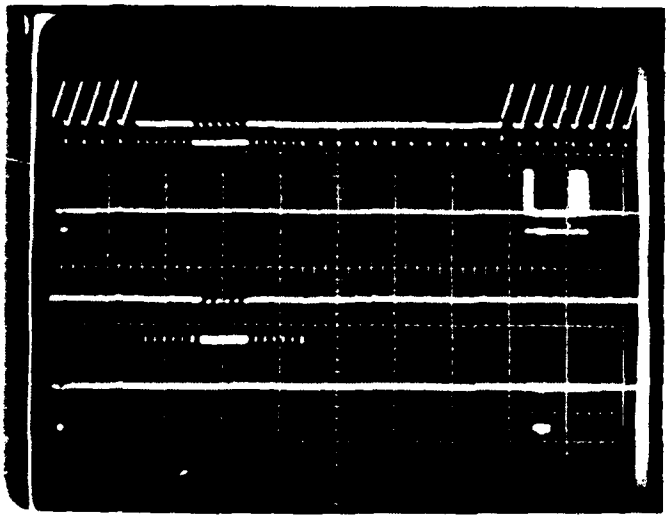


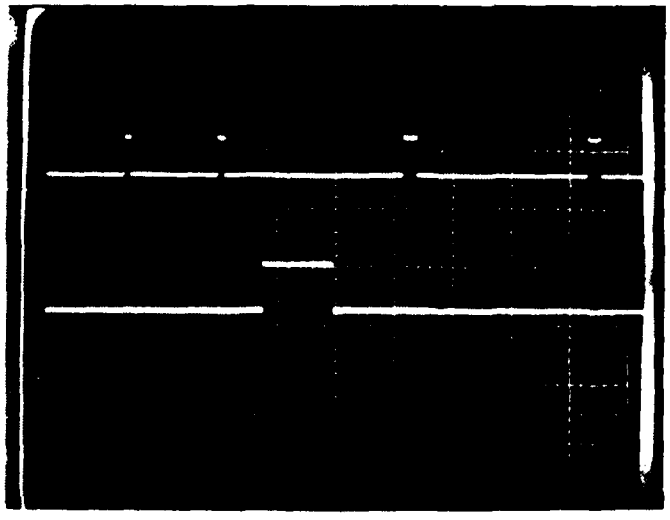
Figure 3.5 Sync Stripper



1v/cm
LPF
VIDEO

5v/cm
VERTICAL
SERATIONS
(A72-G)

200 μs/2ms (a)



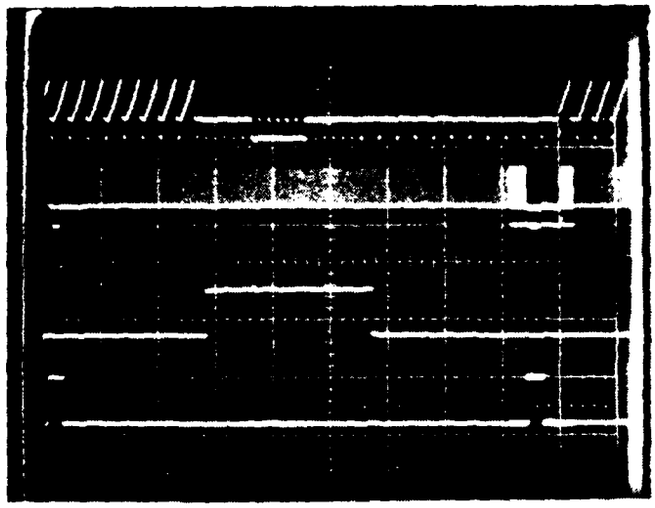
A72-10

FIELD
#2

A72-9

20 μs (b)

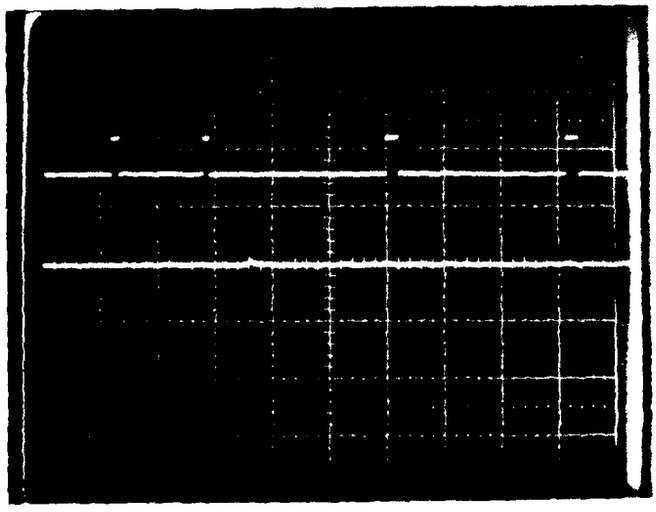
Figure 3.6 Sync Separator Waveforms



1v/cm
LPF VIDEO

5v/cm
VERTICAL
INTERVAL
(A92-13)

200 μs/2ms (c)



A72-19

FIELD
#2

A72-8

20 μs (d)

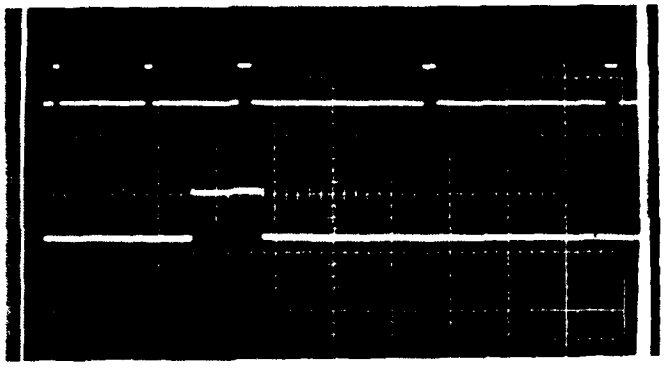
Figure 3.6 Sync Separator Waveforms (Continued)

inputs to the gate which result in no output during field number 2. Figures 3.7A and 3.7C demonstrate the output pulse obtained from the gate during the start time of field number 1. By stretching field 1 pulse to equal one line (62.5 us) the pulse called "New Frame" is produced as shown in figure 3.7B.

There are two phase-lock loops which are used to produce the high frequency system timing clock for system operation when live or taped analog video is used as the system's input source. It is characteristic of several helical scan recording systems to produce a dead spot during vertical sync where no horizontal pulses occur. Standard digital frequency comparators would instantly detect the missing pulses and interpret a rapid change in frequency thereby causing the phase-lock loop to produce unwanted frequency shifts in the output. To eliminate this problem a ramp and hold phase detector was designed which will maintain a constant output frequency when a few input horizontal pulses are missing.

Figure 3.8 is a block diagram of the first phase-lock loop. The voltage controlled oscillator A79 has an output frequency of approximately two times the horizontal line rate when the phase-lock loop is open. The output of the voltage-controlled oscillator (A79) is divided by two and the output is formed into a narrow pulse (A80,A90). The output pulse is then used to trigger a ramp generator to produce a linear ramp as shown in the figure. The ramp generator provides the signal source for a sample and hold circuit which is sampled by the horizontal sync signal from the horizontal pulse former (A78). The sampled amplitude of the ramp is then low-pass filtered and is used as the control voltage to the voltage-controlled oscillator. The output frequency of the voltage-controlled oscillator is modified to the proper frequency to produce the ramp as shown in the figure. If a few sampling pulses are missing, the output of the sample and hold will remember the laser amplitude sampled and the output of the VCO will remain constant.

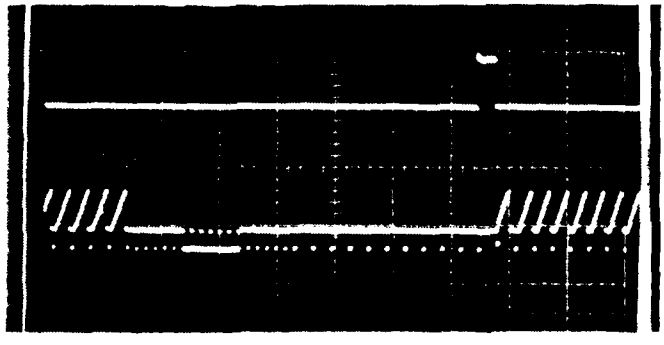
The second phase-lock loop is used to generate the high frequency clock which is used to generate system timing when analog video is used as the system's input. The output of the first phase-lock loop provides the reference signal to the digital comparator which is used in the second



A72-10
A72-9

FIELD 1
GATE PULSE

20 μs (a)

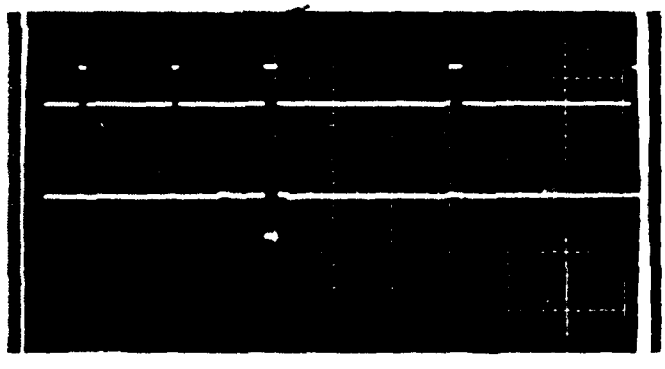


A4-11

NEW FRAME

LPF
VIDEO

200 μs (b)



A72-10

A72-8
FIELD 1
PULSE

20 μs/5ms (c)

Figure 3.7 Sync Separator Waveforms

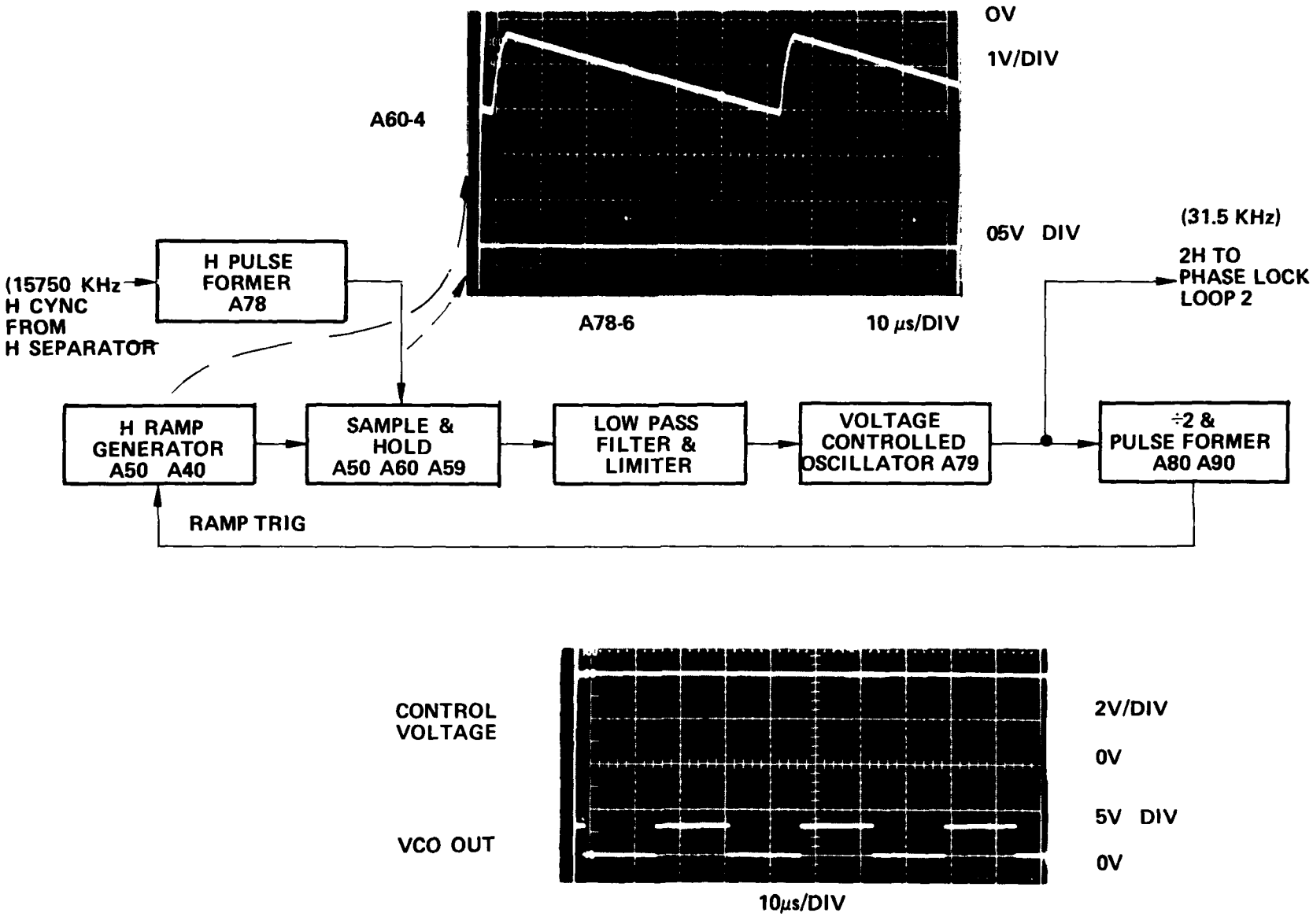


Figure 3.8 Phase Lock Loop #1

phase-lock loop as shown in figure 3.9. The second input to the comparator is provided by a divider chain from the high frequency voltage-controlled oscillator. The output of the comparator is low-pass filtered and provides the control voltage to the voltage-controlled oscillator. The output of the voltage-controlled oscillator is 1216 times the horizontal rate of the video or approximately 19.152 MHz.

When the system is under computer control or when there is no sync present on the input video, a 20 MHz crystal oscillator is used to provide the clock to the timing circuits. Figure 3.10 is a block diagram showing the sync detector and the automatic switching circuit so that the memory is always provided with a stable clock. The basic memory circuit is a dynamic ram and continuously needs refreshing to maintain its contents.

3.5 DIGITAL DEFLECTION GENERATOR

The sweep waveforms to the high resolution cathode ray tube are digitally generated to ensure the accuracy of the deflection signal. The circuitry which is used to provide the ramp waveforms also provides the necessary blanking and synchronizing signals when the system is used with an internal clock source. The system uses both horizontal and vertical interval counters along with digital-to-analog converters to produce the output analog waveforms. The output of the vertical digital-to-analog converter is summed with a square wave so that the output image will be properly formatted. The output of the deflection generator also includes composite blanking, vertical blanking, V square waveform, New Frame, and Mid Frame signals (where New Frame and Mid Frame are signals used by the memory control circuits).

The selected clock signal is used as the input clock for the horizontal counters which are programmed to divide the clock by 1216 as shown in figure 3.11. The horizontal counters are synchronized to external horizontal sync when the system is used with an analog input through a pulse forming circuit. The output of the horizontal counters provide the 10-bit input to the digital-to-analog converter as well as the horizontal blanking output. The output of the digital-to-analog converter is amplified and buffered to provide the ramp input to the cathode ray tube.

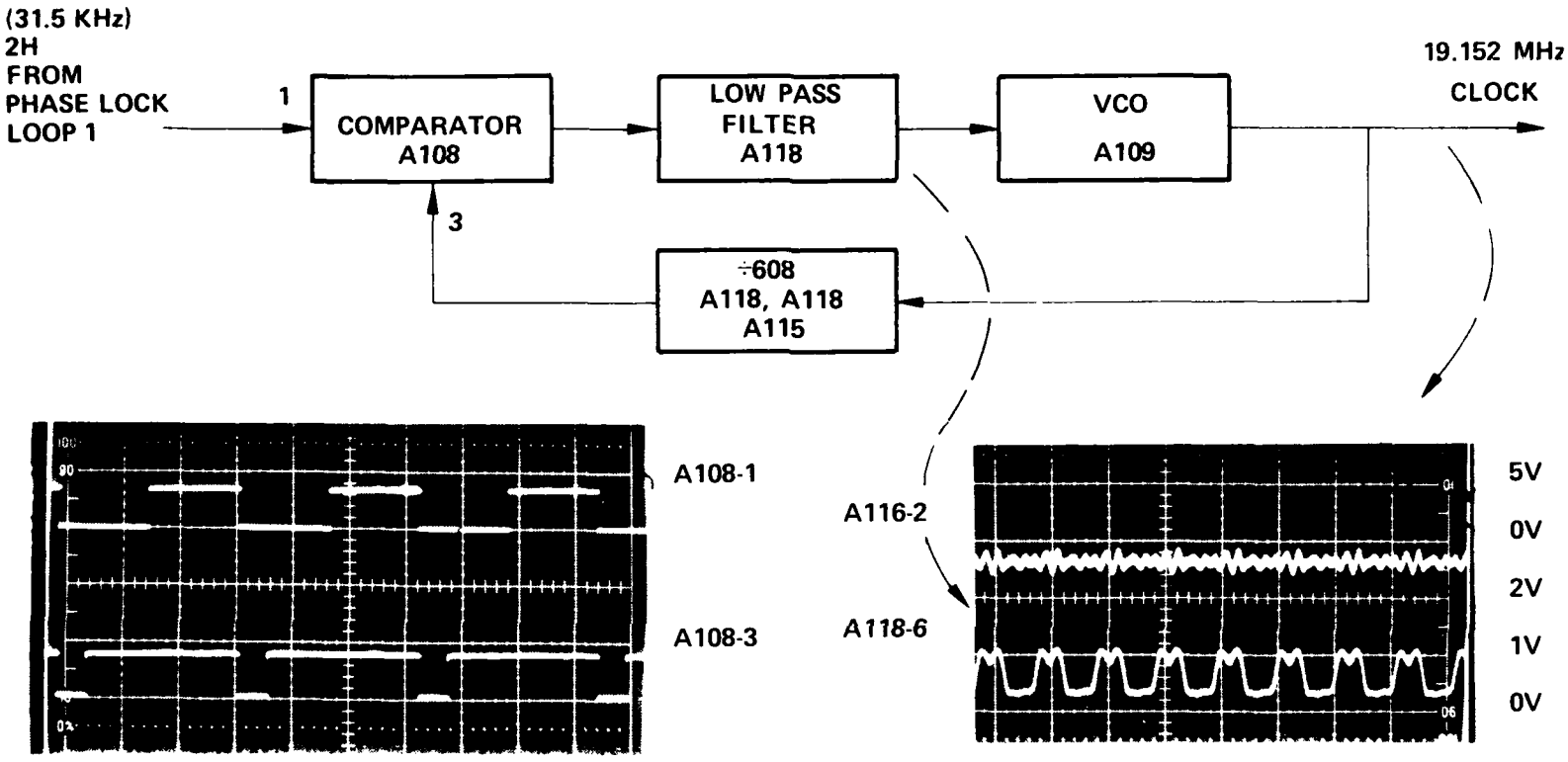


Figure 3.9 Phase Lock Loop 2

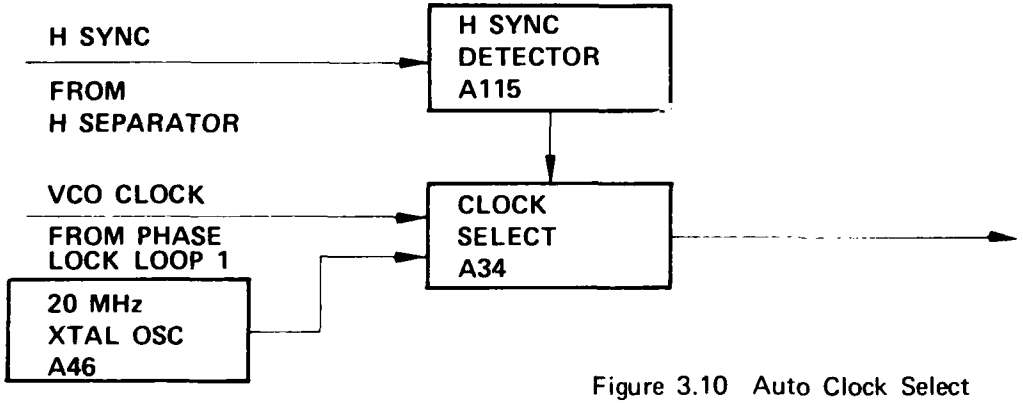


Figure 3.10 Auto Clock Select

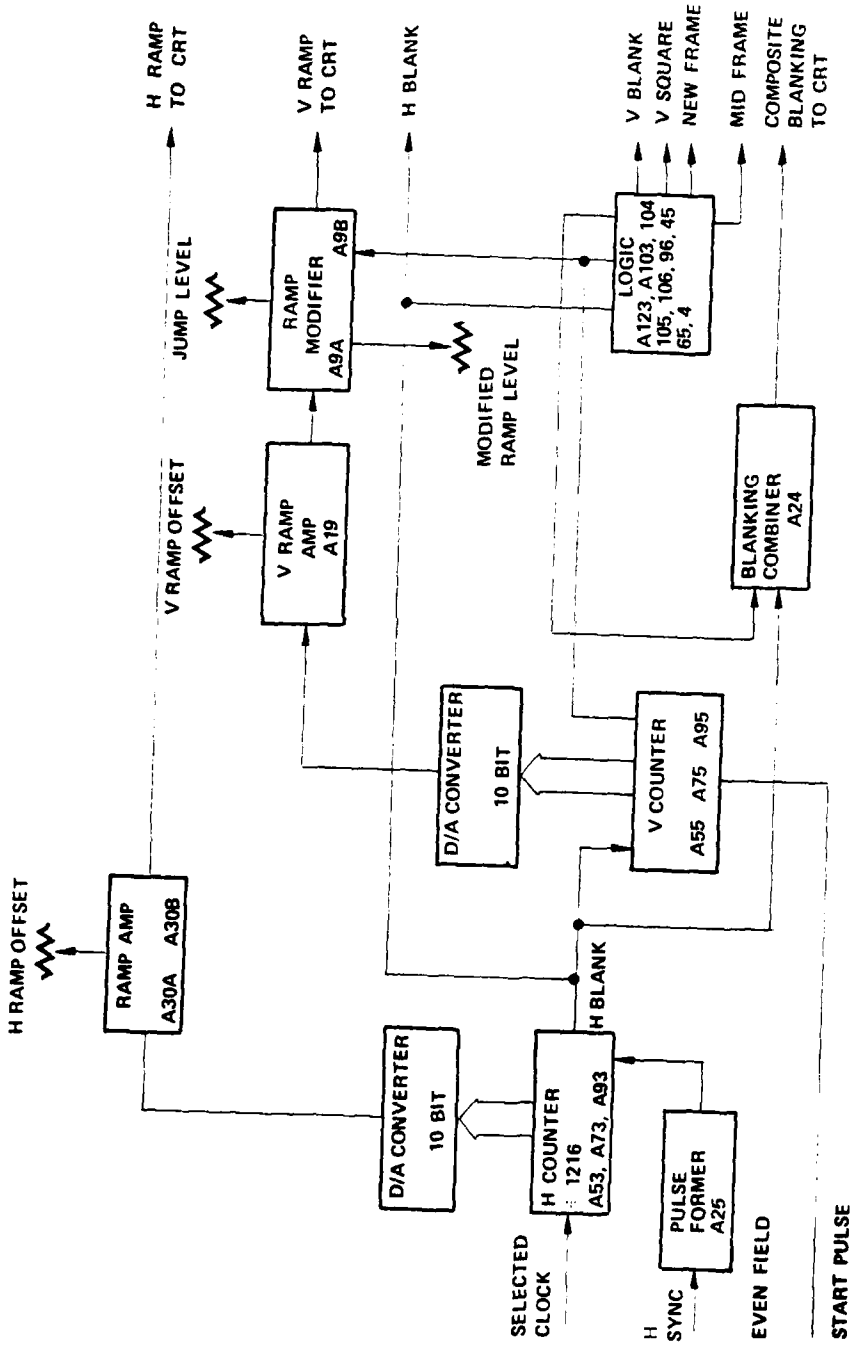


Figure 3.11 Digital Deflection Generator

The horizontal blanking signal is also used to clock the vertical counter which provides the 10-bit ramp information to the vertical digital to the digital-to-analog converter as well as the vertical blanking and square wave which is used to modify the vertical ramp. The vertical ramp from the digital-to-analog converter is amplified and summed with the provided square wave signal from the vertical counters. Both the square wave and the ramp waveform have a period of one video frame. The vertical counters are also externally synchronized by the even field pulses produced by the sync stripping circuits described in previous sections.

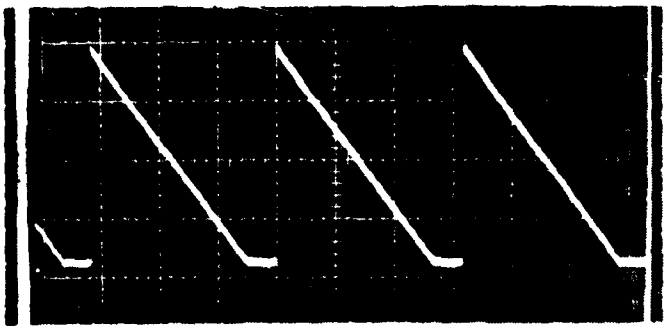
Figures 3.12A, 3.12B show the output waveforms of the digital waveform generator and figure 3.12C is the raster format which results from providing the oscilloscope with the generated signals to the X and Y inputs respectively.

3.6 FRAME STORE MEMORY AND CONTROLLER

The frame store memory is divided into two sections as shown in figure 3.13. Each section of the memory stores one field of the input video information. Since it is possible to write each section of the frame store memory independently, individual image sources can be stored.

The memory output is used to refresh the high resolution cathode ray tube in the proper format for joint transform correlation. This is accomplished by properly timing the read sequence. The output of the memory is also interfaced to the digital computer for storage on digital tape. Signals stored on digital tape can also be transferred to the frame store system. The computer timing is not interactive and video information to the CRT will be lost during computer access times.

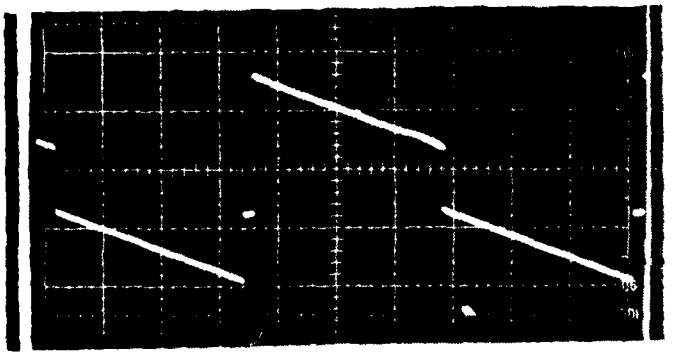
There are seven multiplexed address lines which define the location of stored information within a memory chip (A0-A6). These multiplexed addresses are strobed into the memory by the row address strobe (RAS) and the column address strobe (CAS). The control signals to the memory card are organized to accomplish multiplexing of the input data to increase the memory system capability. CAS 11, 12, 13, and 14 control one half of the card which has been subdivided into four sections. CAS 21, 22, 23 and 24 are the corresponding control signals for the other half of the memory



H RAMP

.2v/div.

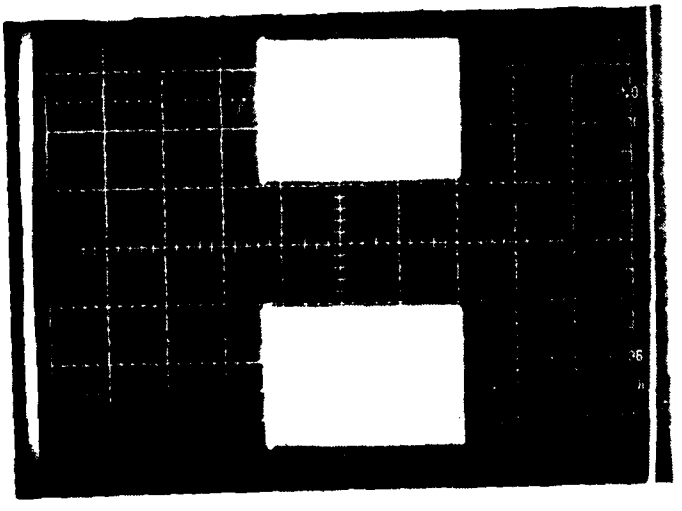
20 μs (a)



V RAMP

.2v/div.

5 ms (b)



(c)

X Y DEFLECTION
H → V ↑

Figure 3.12 Deflection Generator Waveforms

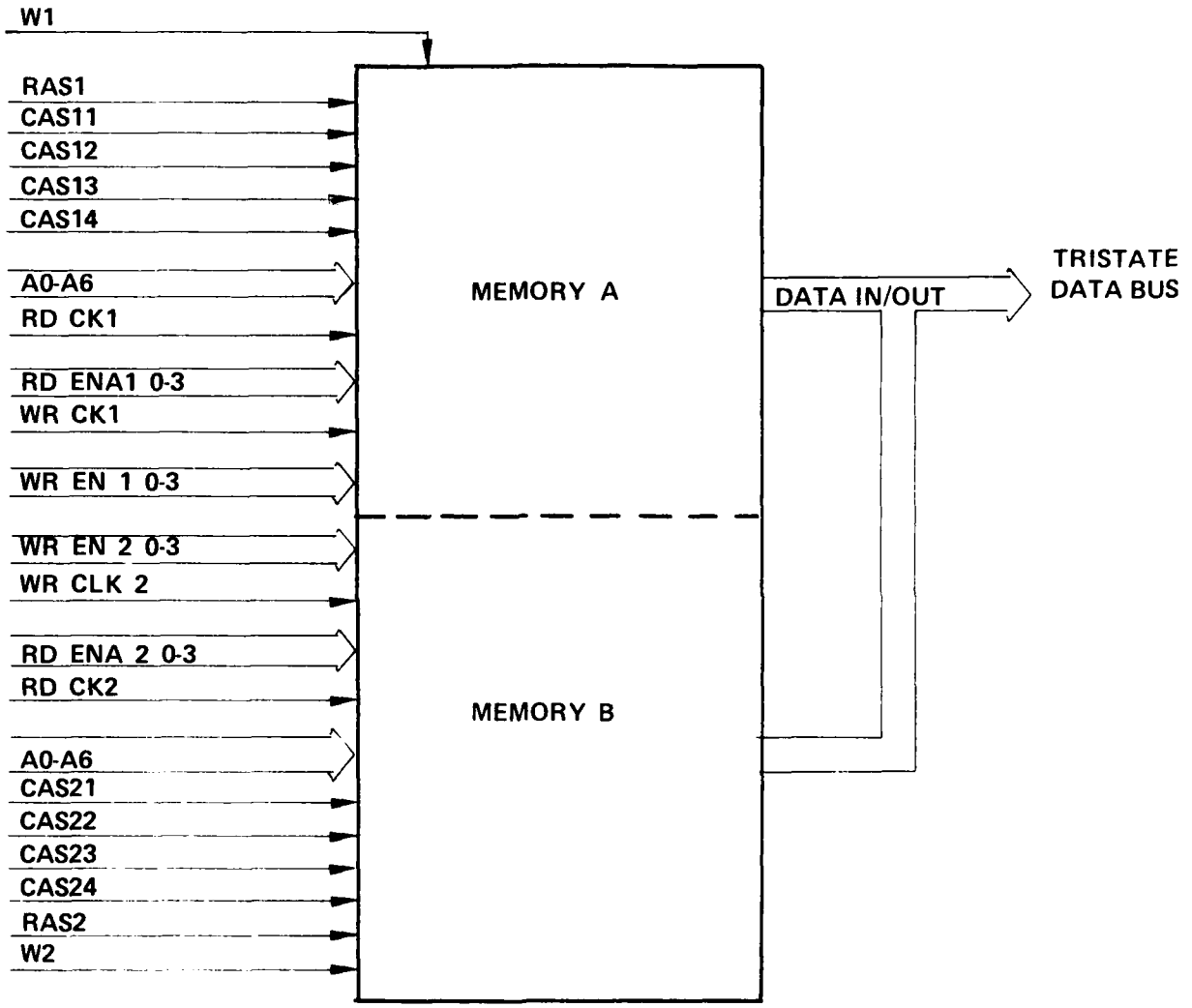


Figure 3.13 Frame Store Memory

card. The write enable (WR EN) signal controls the data in/out function of the memory card's input logic. Where the write clock (WR CK) strobes the data into the memory card input latches. The write (W) command input to the main memory allows writing the latched input data into memory locations determined by the address to the memory chips.

The read clock (RD CK) signal latches four pixels in a parallel manner into the memory card's output latches. The read enable (RD EN) controls the data in/out function of the memory card in/out latches in a sequential manner such that the four latched pixels are distributed to the video bus sequentially.

The memory system when properly controlled will produce two fields of video information each having a format of 256 X 256 pixels with an 8-bit amplitude resolution (256 levels).

The frame store sequencer is used when storing analog input video information and when the frame store is used to refresh the cathode ray tube system. A block diagram of the frame store sequencer is shown in figure 3.14. The selected clock input is from the phase-lock loop system when digitizing and storing analog input video information. The clock is divided to generate a 3-bit address line to the timing pulse generator. The timing pulse generator is an integrated circuit which is used to decode one of ten input addresses; however, only one of eight is being used in the sequencer. The timing pulse decoder is an arrangement of set reset latches which appropriately produce the proper pulse timing to the frame store system. The output of the timing pulse decoder is passed through Tri-State logic to enable the selection of computer or real-time control. Decoded manual control panel logic is used to determine what frames are to be stored and in what area of the memory. The frame store sequencer is completely synchronized with the input video signals through the proper use of horizontal and vertical timing signals.

The mini memory sequencer showin in Figure 3.15 is operated through the minicomputer interface and provides one sequence for writing or reading the memory for each input command received. The clock source for the timing circuits is always provided from the 20 MHz crystal oscillator contained in the system. The 20 MHz signal is appropriately divided to

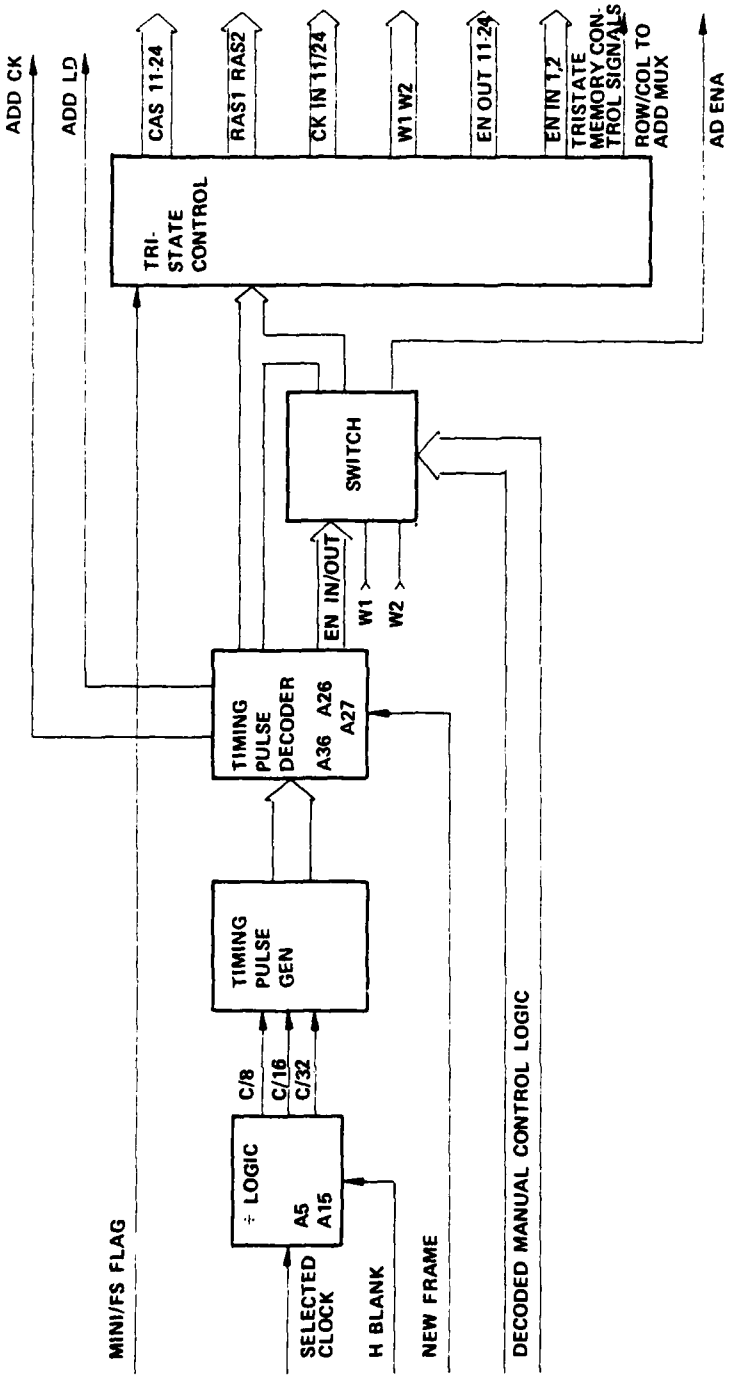


Figure 3.14 Frame Store Sequencer

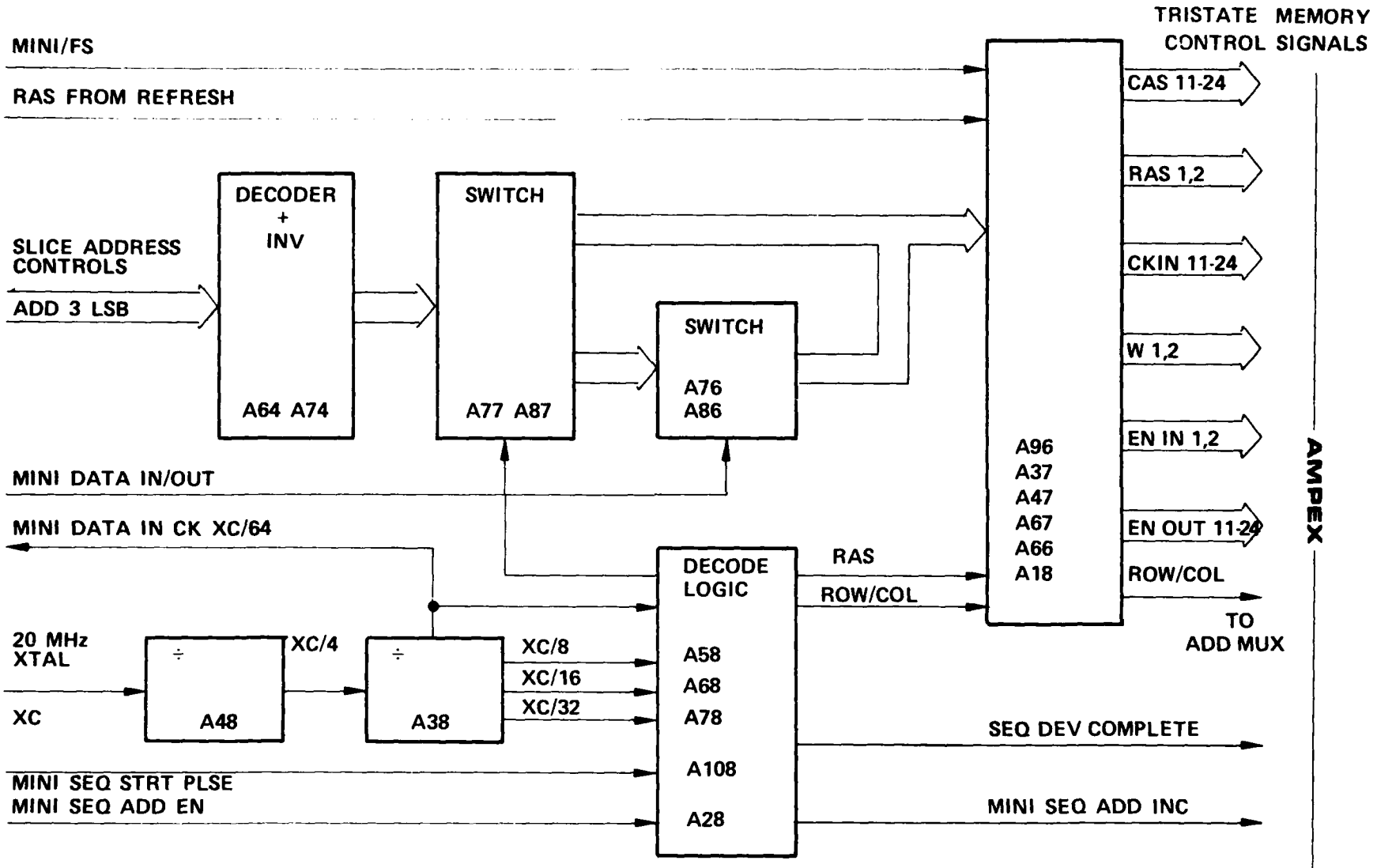


Figure 3.15 Mini Memory Sequencer

provide a 3-bit address to the decode logic where the proper memory waveforms are generated.

For pixel access from the memory or for writing a single pixel into the memory, the three least significant address bits from the computer interface are used as the read enables (RD EN 1 through 4) or the write clock lines (WR CK 1 through 4) of the appropriate memory section determined by the computer interface address the most significant bit.

The address generator for the computer system consists of two address counters, one for the minicomputer and the other for normal frame store sequences. Each of the address counters are connected through Tri-State logic so that either source can be used for the operation of the memory system. The total number of address lines for the system is 17. The three least significant bits of the address are used for slice control. Slice control defines what section of memory chips are being selected for use through the CAS lines or input WRITE clocks or READ enables. The most significant address bit is used for determining which field is to be stored in which half of the memory. 14 of the address lines are used as the input to the address multiplexer where the address information is time multiplexed with respect to the RAS and CAS signals which have been previously defined. The resulting 7-bit address line is used to determine where the memory chip is being accessed. The Block diagram of the address generator is shown in Figure 3.16.

Figure 3.17 is a block diagram of the logic controlling the data in/out function from the computer interface. The logic also provides an automatic access of the minicomputer to the frame store which can be overridden manually with an on card switch.

The computer interface which is used with the system allows the operator to load the frame store from a digital tape. The interface also allows the generation of a digital tape from the frame store memory. The block diagram of the computer interface is shown in Figure 3.18. The proper sequence of commands from the computer causes the necessary addresses and data to be latched for exercising the frame store memory system.

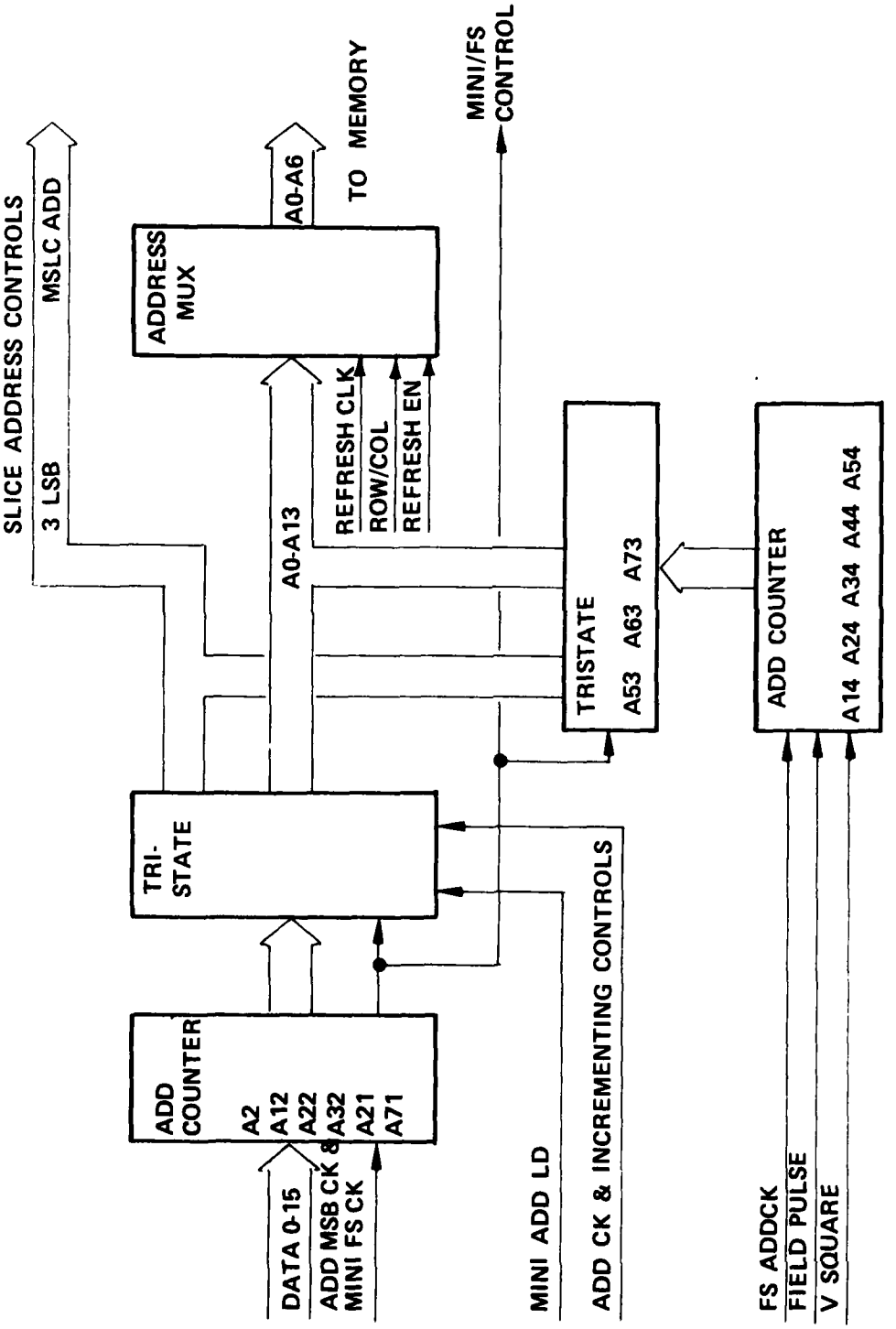


Figure 3.16 Address Generator

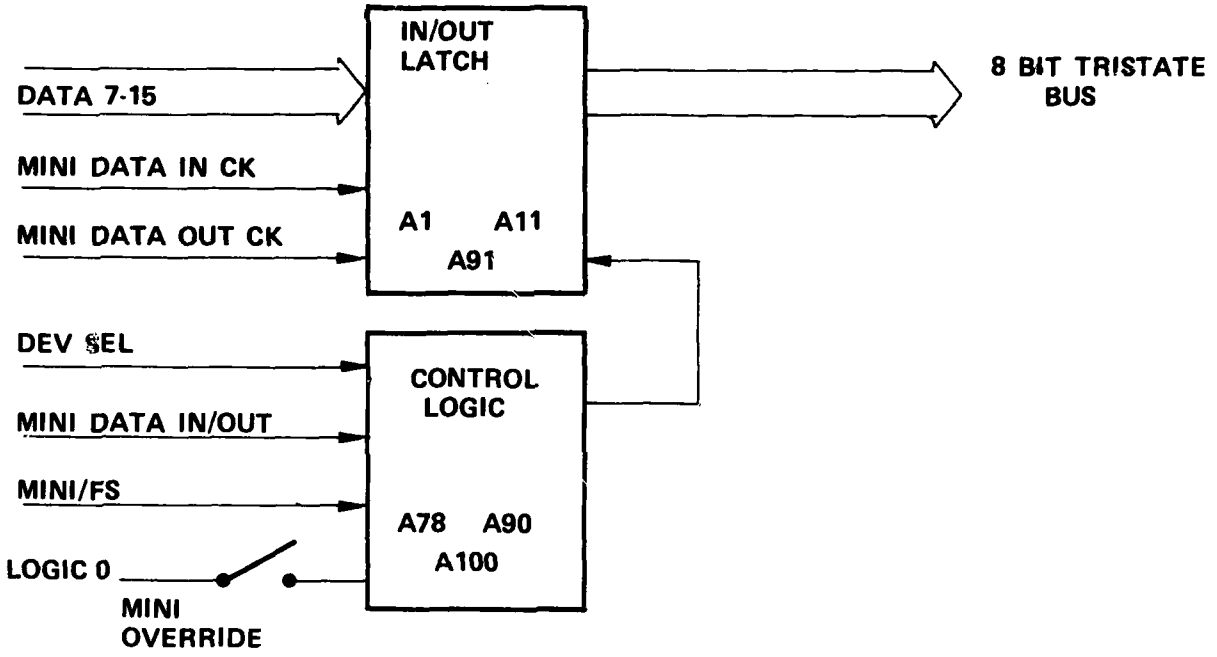


Figure 3.17 Computer Data In/Out Control

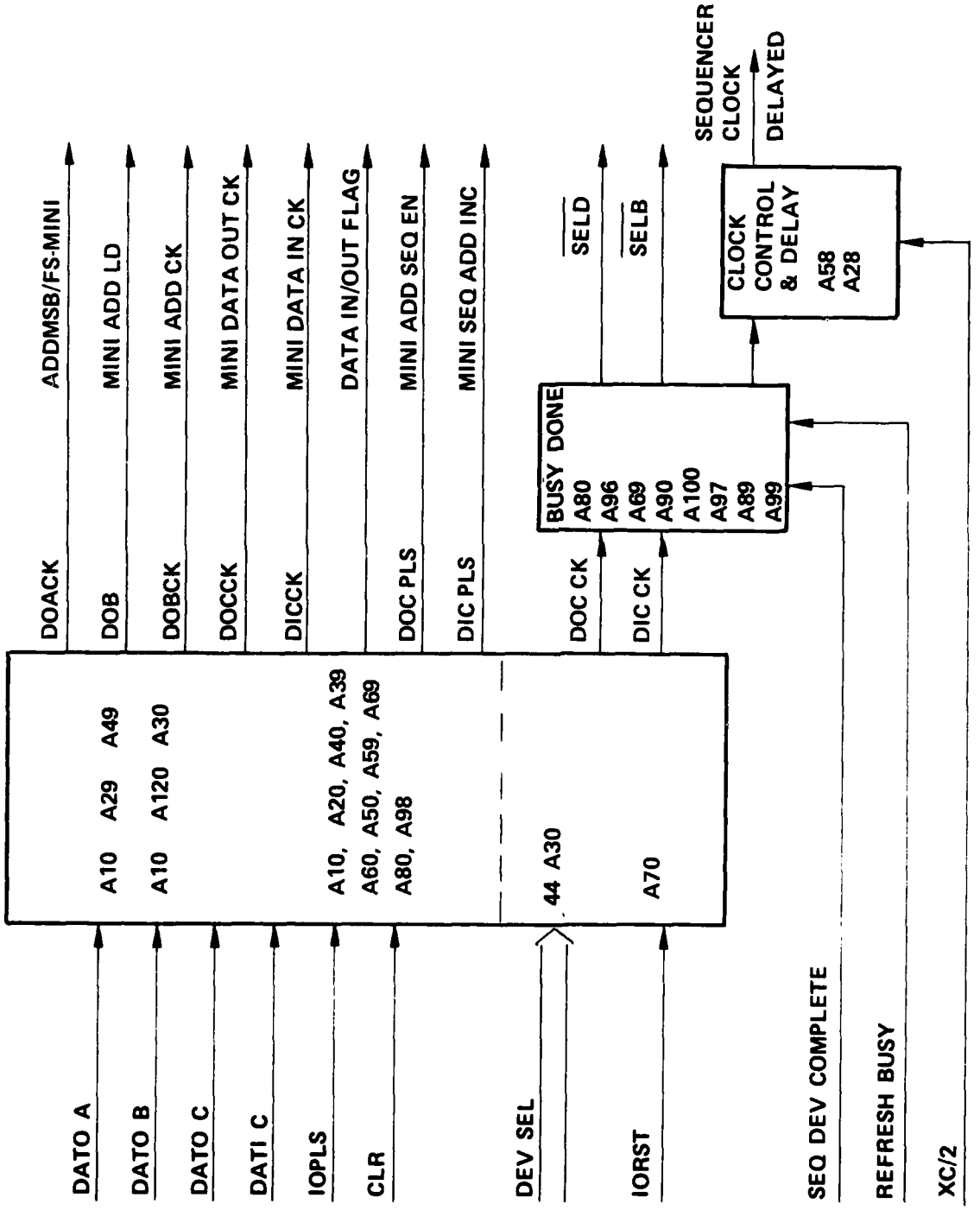


Figure 3.18 Computer Interface Control Functions

The frame store interface is device 44 and is called from the system software. A device select and a DATO A command produces the DOA clock which latches the memory address's most significant bit and the frame store/mini command which are on the DATA lines from the computer. The second device select with a DATO B command produces two signals in sequence to hatch the remainder of the address. The first signal produced is DOB which provides the mini address load, a signal which enables address latching. The second signal produced from DATO B is a DOBCK which is the address load clock. The first two sequences provide the mini frame store signal and the address in the frame store where the data is to be written or accessed. The third computer command DATO C produces a series of signals in the interface which first cause the data from the minicomputer to be latched in the data input register (DOCCK=mini data out ck). The mini data out clock will also start the mini data sequencer so that the latched data is transferred to the frame store at the specified address. If a sequential data stream is to be entered into the frame store, the IOPLS from the computer is gated with the DATO C command to produce the mini address sequencer enable (mini addseqen) flag. When this flag is set it is not necessary to repeat the DATO A and DATO B commands since the interface address counter is stepped after each DATO C command from the computer. The DATO C command also sets the interface logic which determines which data is to be transferred from the minicomputer to the frame store system (DATA IN/OUT FLAG). To read data from the frame store the first two command sequences are repeated to set the proper address location in the frame store (DATO A and DATO B). The third command for reading the frame store is the DATI C command which resets the mini data in/out flag, starts the mini frame store sequencer, reads the previously latched data from the frame store into the computer, and latches the output of the frame store for the next frame store read command. If a sequential string of data is desired from the frame store, DATI C is gated with the IOPLS to produce a signal which increments the interface address counter before the mini sequencer is started so that the data corresponds to the address start point which has been latched.

Since the frame store memory uses dynamic random access memory, a refresh clock is required when the system is under computer control. The refresh cycle is made transparent to computer operations since all of the

data and addresses have been latched into the interface. If the memory is not in the refresh cycle during a computer cycle, the system operates as previously described. If the refresh timer clocks to a refresh command during a mini frame store sequencer cycle, the refresh is held off until the cycle is completed. If the refresh cycle is busy when the command is given to enable the mini frame store sequencer, the sequencer will not cycle until the refresh cycle is completed. The computer DATO C and the DATI C commands set the busy flag and the flag will indicate busy until the sequencer has completed its cycle. If the refresh cycle is running, the data and addresses can still be latched into the computer interface, but if the sequencer is operating, the busy flag is set and new data should not be latched.

For running the frame store with an analog input video signal a manual control panel has been provided. The control panel uses a rotary switch to set the format which is to be used and a group of push button switches which enable the write logic. The push button switches are synchronized with the video vertical sync information. The output of the rotary switch is decoded and is used as control logic to the frame store sequencer. The block diagram of the manual control logic is shown in figure 3.19.

A block diagram of the refresh control circuit is shown in figure 3.20. The refresh control is used only when the computer interface is activated. The input signals to the refresh control circuit provide for synchronization via internally generated H blanking and New Frame. The busy flag is provided as an input to prevent the refresh clock from turning on during a computer frame store access cycle. A clock is provided as the input to the refresh controller time base and all refresh periods are derived from this clock. The output of the refresh control circuit is the refresh device complete, refresh enable, and the refresh clock which is only active during the refresh cycle.

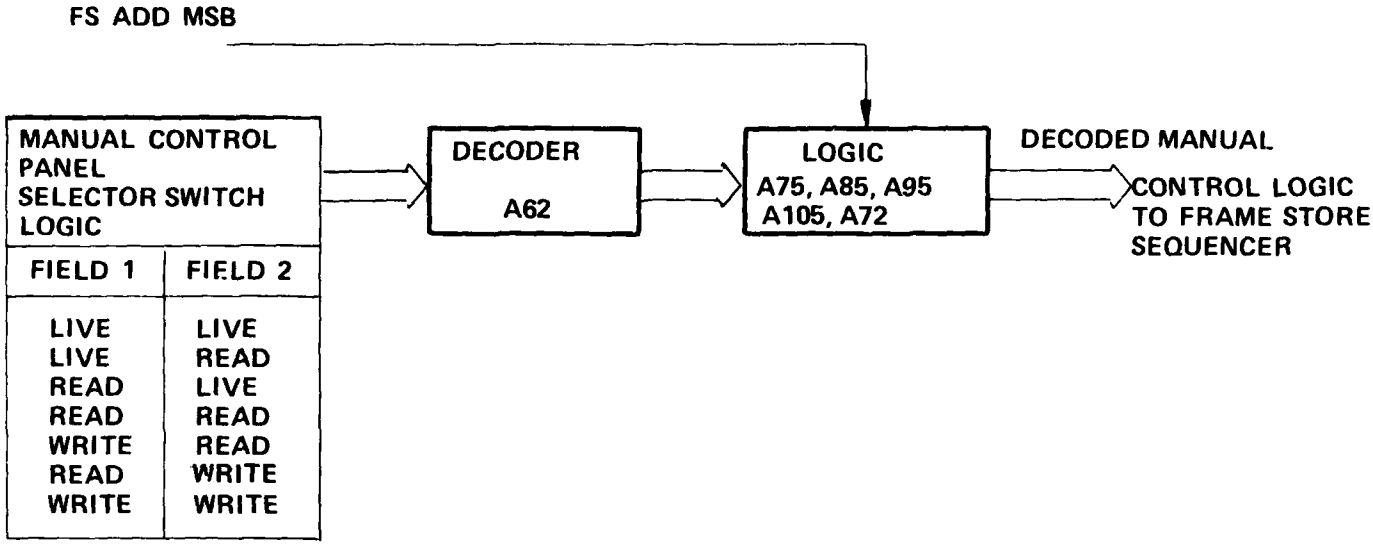


Figure 3.19 Manual Control Logic

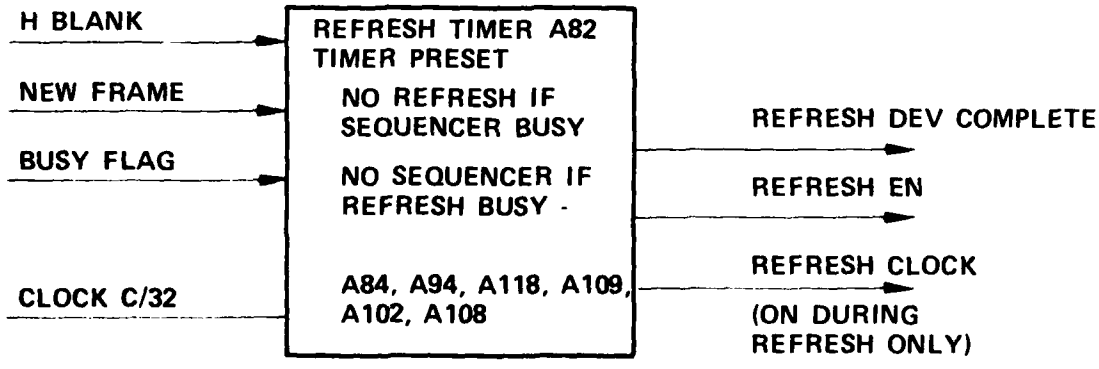


Figure 3.20 Refresh Control

3.7 INPUT/OUTPUT VIDEO PROCESSING

The filtered input video signal is converted to 8-bit digital words using a 5 MHz clock signal. The input signal processing to the A/D converter level shifts and clamps the video to a level which is appropriate to the requirements of the converter integrated circuit. The clamping is accomplished during the back porch interval of horizontal sync and the DC level of the clamp is such that transitions which are negative with respect to the clamp are not digitized. Figure 3.21 is a block diagram of the A/D and the D/A converter interconnection as the components are used in the system. The output of the A/D converter is passed through a Tri-State switch to the Tri-State data bus. The switching logic is controlled by the DATA IN/OUT logic from the frame store sequencer to prevent more than one output device from being on the Tri-State bus at one time.

The A/D converter is continuously tied to the Tri-State data bus and receives both a 5 MHz clock and a horizontal blanking signal. The horizontal blanking signal produces a zero output during horizontal blanking. The output of the D/A converter is low-pass filtered and and produces the signal for the video processing circuit shown in figure 3.22. The video signal is divided into two paths. In the upper path in the block diagram the video is buffered, filtered, and amplified and is used as the signal source to the cathode ray tube through the system's patch panel. In the lower path the video is amplified, filtered and buffered into a mixer circuit where upper and lower sidebands of the video are generated on a 2 MHz suppressed carrier. The upper sideband is filtered, amplified, and passed to the CRT through the system patch panel.

Using single sideband suppressed carrier techniques in passing the video to the optical system introduces an offset of image frequency components at the joint transform plane of the optical system. The spatial offset at the joint transform plane moves the low spatial frequency components away from the zero order and makes it possible to enhance output correlation of the low frequency components. Due to the spatial frequency response of the liquid crystal light valve/cathode ray tube, the high frequency components may suffer decorrelation.

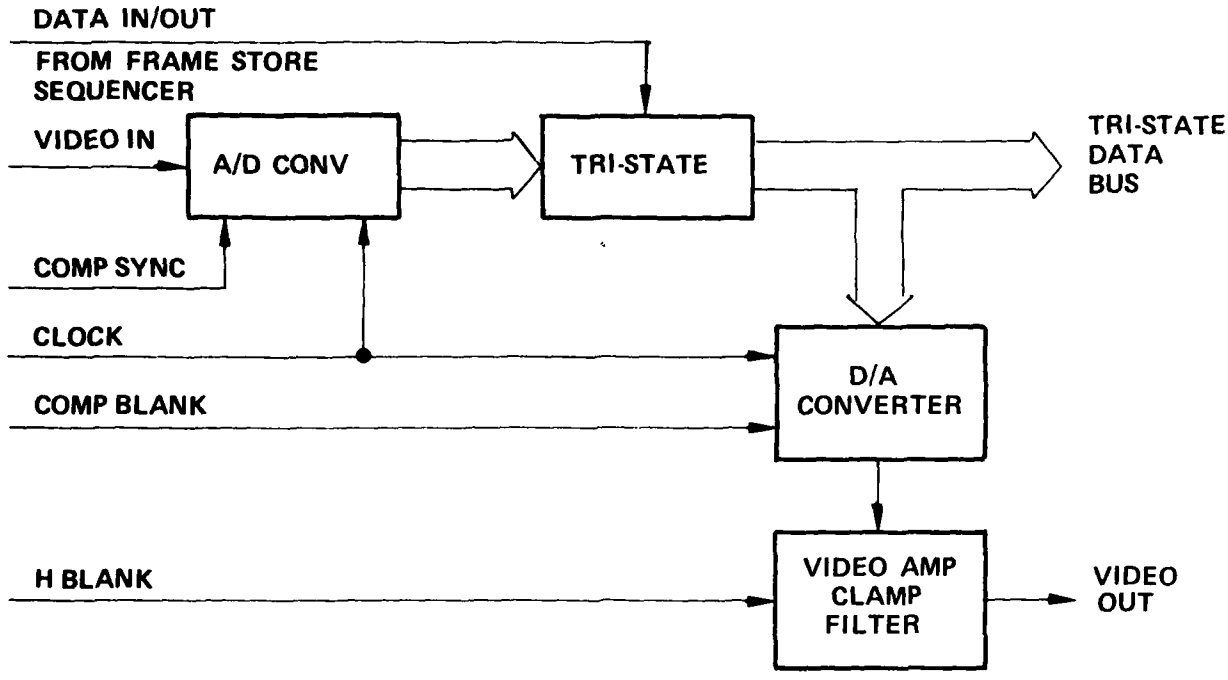


Figure 3.21 A/D D/A Converter

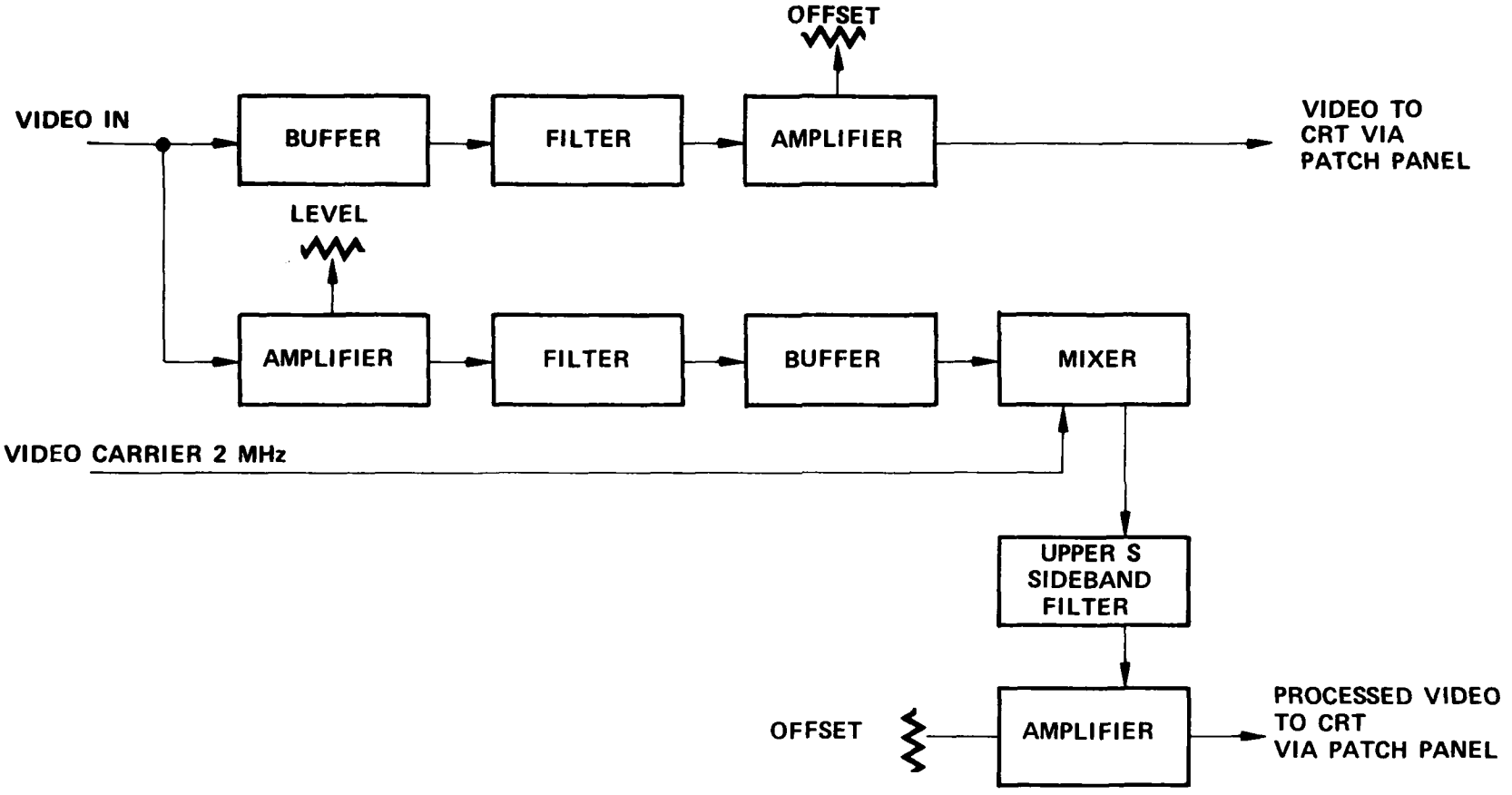


Figure 3.22 Video Processor

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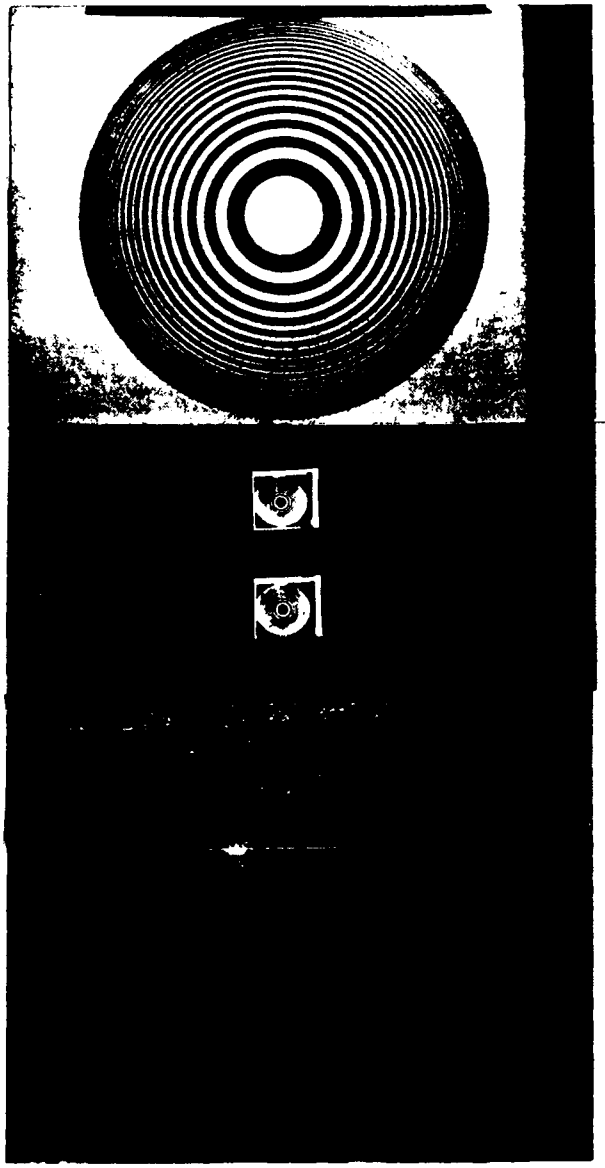
4. SYSTEM PERFORMANCE

Due to time limitations there were only limited tests performed on the joint transform correlator system.

Test images are detected by a vidicon camera digitized and stored in the frame store system. The stored images can be read to the cathode ray tube in various combinations of stored or live information for fully evaluating the system's ability to crosscorrelate information contained in two separate images. Although not fully tested the effects of scale and rotational changes could be evaluated.

A test image which has excellent compressing capability was used to roughly evaluate the dynamic range of the system. The Fresnel image which was used for the system input is shown in figure 4.1a. This image was stored in both fields of the memory. The cathode ray tube input transducer to the optical bench was refreshed from the memory in the format as shown in figure 4.1b. The resulting correlation output is shown in figure 4.1c as detected by a vidicon camera and is displayed using the output video support system. Other output video system displays which are used include an isometric (3D) display as shown in figure 4.2a, and an "A" scope display of a line section of the output video as shown in figures 4.2b,c. Figures 4.2b and 4.2c can be used to partially evaluate the system's dynamic range since 4.2c is the output of the optical system with the cathode ray tube image removed. The dynamic range of the system is approximately 32db.

Figure 4.3 shows the effect of motion of a live image with respect to a fixed image which is stored in the frame buffer. The cathode ray tube image is shown with the respective 2D and 3D output correlation peaks. Figure 4.4 demonstrates the use of characters as the input image with the corresponding correlation peaks from the 3D display.



INPUT
TEST
TARGET

(a)

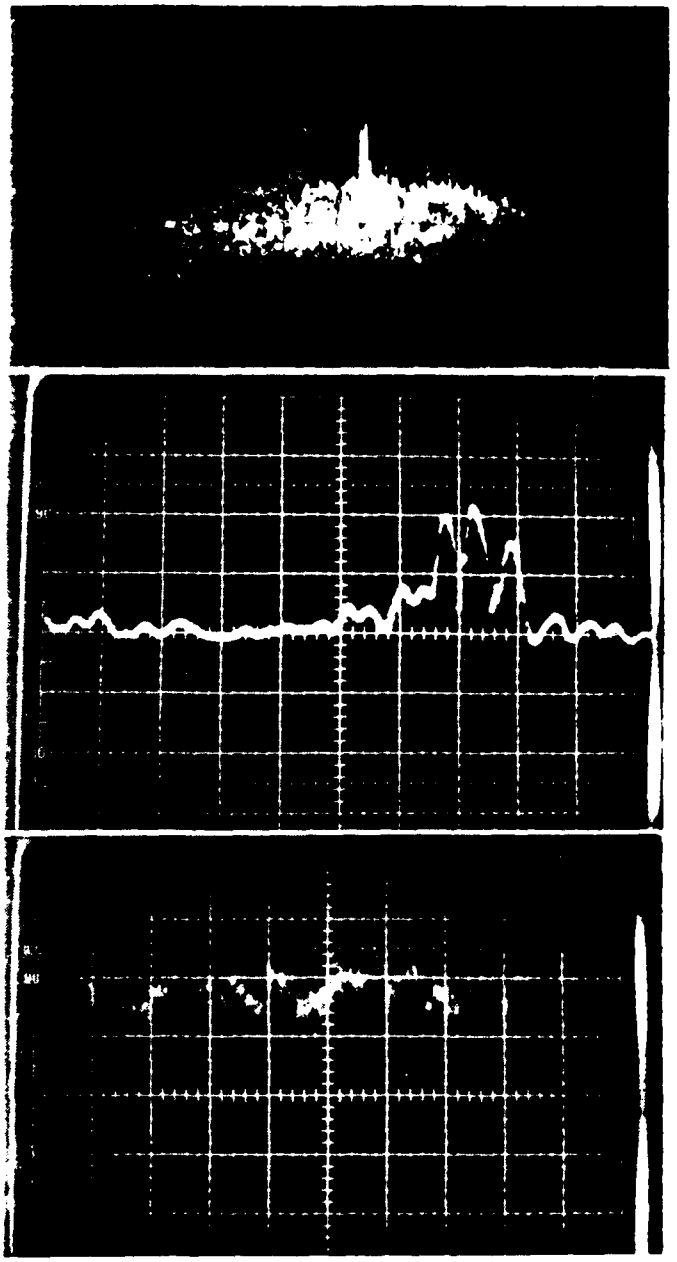
CRT INPUT
IMAGE

(b)

CORRELATION
OUT

(c)

Figure 4.1 System Test



ISOMETRIC
CORRELATION
OUT

(a)

A SCOPE
VERTICAL
.5v/cm
HORIZONTAL
1 μs/cm

(b)

A SCOPE
VERTICAL
50 mv/cm
HORIZONTAL
1 μs/cm

(c)

Figure 4.2 System Test

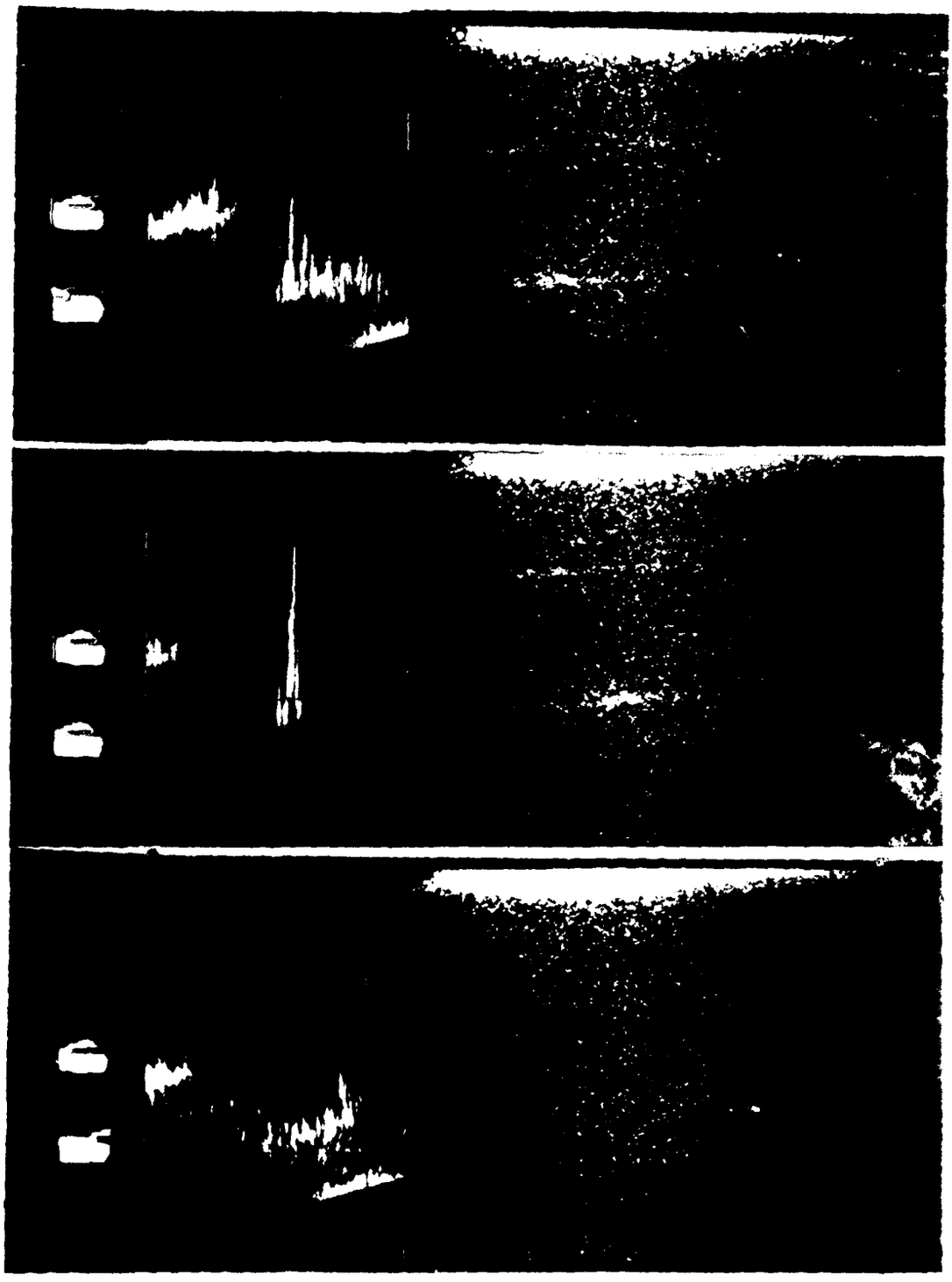
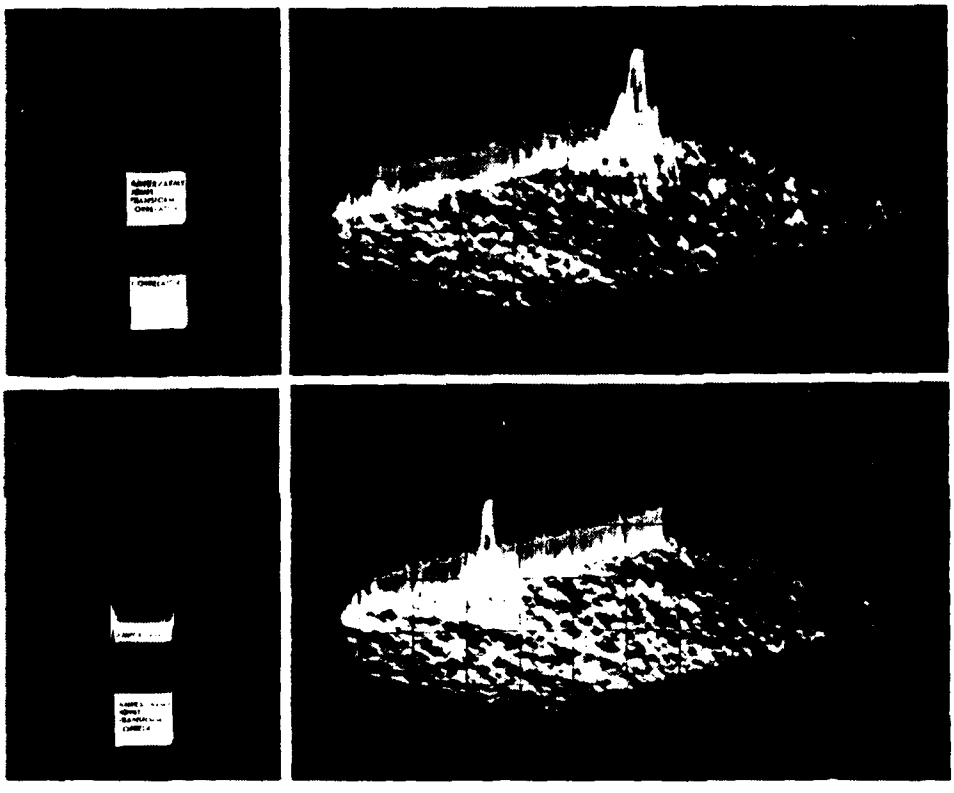


Figure 4.3 System Test

(a) (b)



(c) (d)

Figure 4.4 System Test

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5. SUMMARY

The joint transform correlator system which has been built is a breadboard system which can easily be modified to perform experiments for evaluating alternate techniques employed in optical image processing systems. The ability to modify the optical system in the laboratory will allow the development of new processing techniques as well as developing alternate optical systems for solving common problems.

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